From A 38 mW 12b 100 MS/s Pipelined ADC Design to Less Than a 20 mW One

Mohammad Reza Ghdarei Karkani
IEEE student member
mrghaderi@ece.ut.ac.ir

***Abstract* – A 12 bit pipelined ADC blocks are designed in 0.35 µm mixed-mode CMOS process. The final ADC conversion rate is 100 MS/s while the main circuits consumes only 38 mW power from a 3 V voltage supply. A wide swing gain-boosting technique, is used to design high dc gain and high unity gain bandwidth opamps. Also a technique is presented to reduce the power up to 20 mW.**

I. INTRODUCTION

Analog-to-digital converters continue to play a vital role in virtually all applications ranging from sensor arrays to broadband communication. Power dissipation has always been important, but today is even more so with the emphasis on extended battery life for hand-held multi-media devices [1]. Lowering the power consumption using low power architectures such as SAR architecture is well suited to ultra-low-power application such as monitoring in micro-sensor nodes but it is limited to low resolutions (8 bit) [2]. Achieving both low-power dissipation and high resolution simultaneously requires excellent engineering, new circuit techniques, and architectural innovations [1]. While reconfigurable architectures try to consumes power in order to multimedia application demands [3], some low-power ADCs have been designed using power-saving techniques such as switched opamp and opamp sharing Both operate with the same principle that opamp is active with a half duty during one clock phase [4]. Using architectures which eliminates power consuming blocks such as S/H and first MDAC which require the highest accuracy in conventional pipelined ADC is another technique to reduce power in high-speed high-resolution ADC for highly integrated communication systems [5].

Along with these high demands to reduce the power consumption, significant Impacts of technology scaling on analog circuits design, such as reducing signal swing and intrinsic device gain, require novel solutions and new design techniques. Cascaded amplifier stages have been a popular solution to increase amplifier gain, but they further reduce the signal swings of scaled technology. Cascading several lower gain amplifiers is an alternative method to achieve high gain with reducing in signal swing.

Compensation techniques to stabilize cascaded feedback system, sacrifice the frequency response of the closed loop system to ensure stability. Although, recent development in the area of pipelined ADCs avoids these problems by using open-loop amplifiers with digital calibration to compensate for the gain variation [6], optimum designs in conventional methods in addition with some enhancement techniques, always show performance not necessarily less than innovative designs.

In this work a conventional Pipelined ADC architecture is selected to design a 12b, 100 MS/s ADC in 0.35 µm mixed-mode CMOS process. A telescopic cascode amplifier and a wide swing gain-boosting technique are used to design high dc gain and bandwidth opamps for higher linear stages.

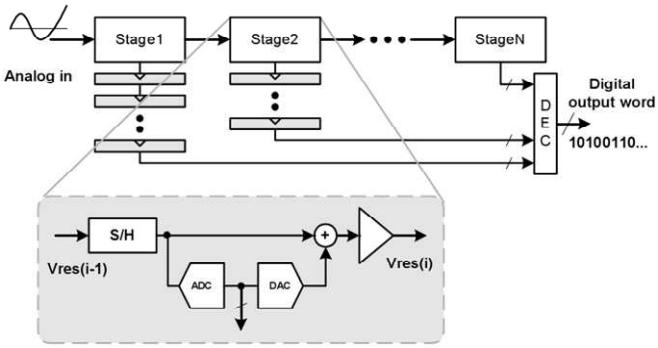

Fig. 1. The block diagram of a pipelined ADC.

The pipeline residue stages are scaled down to reduce both power and area while in each stage the low power opamp design was the main goal. The total ADC circuits consumes 38 mW while a method proposed to reduce the power consumption to about 20 mW.

This paper is organized as follow: the next part discusses the pipeline structure. In the third part the opamp circuit design is described. The sample-and-hold and other stage design and the simulation results are coming in the fourt part. In the fifth section the full pipeline structure is reported and a method is proposed to higher reduction in power consumption. Finally the conclusion ends the paper..

II. PIPELINE STRUCTURE

A pipelined ADC consist of a sample-and-hold stage in the front following with some residue stage each of them generating some bits based on its characteristics and an analog residue feeding in to the next stage. The block diagram of a pipelined ADC is shown in the Fig. 1. The digital output word is length as long as summation of each stage output bits. Using digital error correction, residue stages most have some overlaps which require more output bits in each stage to correct the opamps and comparators non idealities such as offset and gain error.

A. Pipeline Partitioning

Selecting a pipeline structure depends on some different factors such as power, opamp's gain, linearity and band width, DAC requirement, noise contribution of each stage and latency. One simple partitioning is to divide the whole output bits in to some 1.5 bit/stage residue stage and consider *n* stage for *n* bit resolution. Using several more than 1.5 bit/stage residue stage is an alternative for this partitioning but results in constant linearity for more than 1.5 bit which is not required and usually results in more power consumption. In addition to this, the larger the number of bits per stage, the higher bandwidth and linearity opamp is required so the residue stages

TABLE I
REQUIRED SNDR FOR PIPELINE STAGES

Stage num.	1	2	3	4	5	6	7	8	9
SNDR(dB)	78	66	60	54	48	42	36	30	24

are limited in both accuracy and number of bits. To continuously decreasing linearity and accuracy of stages and so on total power consumption a mixture of different residue stages in pipeline architecture seems to be proper. So in this work to realize a 12 bit resolution a 2.5 bit/stage residue stage is considered for the first stage and eight 1.5 bit/stage are came after it. Finally a 2 bit flash ADC generating the last 2 bit to have 12 bit, considering a half a bit overlap between each following stage.

Having 12 bit resolution, requires more than 74 dB precision in total ADC. Here the SNDR of 78 dB is considered for the first stage. The required linearity of stages decreases about 6dB/bit at each stage in the pipeline. The TABLE I shows the required linearity for each stages in proposed 12 bit pipelined ADC.

B. Input Referred Noise and Stage's Capacitor Calculation

As mentioned in previous part one consideration in pipeline design is the noise contribution of each stage. As the Friis equation indicates that the noise contributed by each stage decreases as the gain preceding the stage increase, the first few stages in cascade are the most critical [7]. So the first stages in pipeline structure most have less noise contribution as the noise of the last stages is attenuated by gain of the preceding stages.

The input referred noise of each stage is approximated as below:

$$\overline{V_{n_{in}}^{\,2}} = \frac{KT}{C_s}\left(4+\frac{0.5}{G}+\frac{16}{G^2}\right) \qquad (1.1)$$

While V_{nin} is the input referred noise, Cs is sampling capacitor, G is the gain of the current stage and KT is a famous constant. Considering different voltage gain for the above equation:

$$\begin{aligned} G=4 &\Rightarrow \overline{V_{n_{in}}^{\,2}} = 5.125\frac{KT}{C_s} \\ G=4 &\Rightarrow \overline{V_{n_{in}}^{\,2}} = 8.25\frac{KT}{C_s} \\ G=4 &\Rightarrow \overline{V_{n_{in}}^{\,2}} = 20.5\frac{KT}{C_s} \end{aligned} \qquad (1.2)$$

The total input referred noise is calculated as below:

$$\sqrt{\overline{V_{n_{in}}^{\,2}}} = \sqrt{\frac{KT}{Cs}\left(\frac{20.5}{2}+5.125+\frac{8.25\eta_1}{4^2}+\frac{8.25\eta_1\eta_2}{4^2\times 2^2}+\ldots\right)} \qquad (1.3)$$

TABLE II
SAMPLING CAPACITOR OF PIPELINE STAGES

Stage num.	1	2	3	4	5	6	7	8	9
Csam (pF)	2	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5

Considering the C_s = 2 pF, including four 0.5 pf, for the first residue stage, a 2.5 bit/stage gain stage, and C_s = 4 pF for the sample-and-hold, the reduction factor of 4 for the first residue stage and 1 for the following stages result in nearly 0.22 mV input referred noise which is less than the V_{LSB} of 12 bit ADC and seems to be proper for this design. The sampling capacitor of each stage is calculated and coming in the TABLE II.

III. OPAMP DESIGN

In order to have high dc gain and high bandwidth opamp the telescopic cascode amplifier is utilized. This opamp is proper for less than 60 dB SNDR stage design as its dc gain is typically limited to 60 dB. The unity gain bandwidth of more than 2 GHz is expected for this opamp configuration which seems to be sufficient for the 1.5 bit/stage residue stages, which show gain of two in feedback and the closed loop bandwidth, could be half of the unity gain bandwidth, about 1 GHz, in this application. Higher dc gain is limited to g_m and R_{ds} of devices, and the unity gain band width bandwidth is limited as the second pole of the opamp reduces the phase margin. Along with this, increasing g_m of input devices result in high power consumption. A popular alternative for higher dc gain amplifier is cascading amplifiers which less restrict the output voltage swing of amplifier, but it consumes high power as the number of stage increases and the speed will be reduced in comparison with single stage amplifiers. The gain boosting amplifiers combine high-frequency behavior of single stage amplifiers with high dc gain of multistage design [8] while consumes less power than multistage amplifier.

A. Telescopic Cascode and Gain Boosted Amplifier

Two kinds of amplifiers are utilized for this realizes different, one a telescopic cascode amplifier for the near end stages which require less than 50 dB SNDR, and the other a telescopic cascode amplifier with two gain booster for preceding stages which require SNDR of higher than 50 db amplifiers. Fig. 2 shows a telescopic amplifier and the nodes where the gain boost amplifier will connect. Two gain boost amplifier are required to boost g_m of both n-channel and p-channel cascode devices called n-booster and p-booster. Using gain boost amplifiers with n-channel input devices for n-booster and p-channel input devices for p-booster, highly limits the swing of the main telescopic amplifier and cause shortcomings in linearity issue. The folded cascode amplifier shows good compatibility with this situation. So a p-channel input folded cascode amplifier is used as an n-booster and an n-channel input one used as p-ooster. The Fig. 3 shows the (a) p-booster and (b) n-booster and the nodes which connect to main telescopic circuits.

B. Optimizing Technique

Dividing the timing budget to two main parts, first, slewing and second, settling time performing the optimum

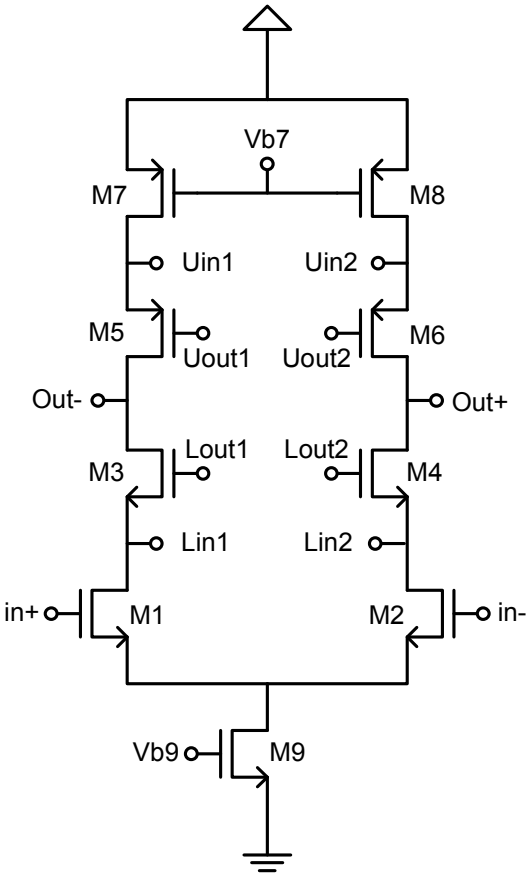

Fig. 2. Schematic of a telescopic cascode amplifier.

power management will be expected. The high slew rate reducing the slewing time but require large bias currents and high power consumption in addition with large devices which increase parasitic capacitance and additionally limits both frequency response and slew rate. As the dc gain of the gain boosted amplifier is not limited and easily reaches 100 db the current is reduced until the slewing time restrict the timing budget for settling time. Increasing the frequency of the amplifiers and reducing the settling time the slewing time increases result in least power consumption. The frequency response of one sample of main boosted telescopic cascode amplifier is coming in Fig. 4, including amplitude and phase for in three corners of.

As the bias circuit of the both Main OTA and the gain boosters some wide swing current mirror used which uses a reference current source to generate the bias voltages.

C. Switching Common mode Feedback

For both main Telescopic cascode OTA and the gain booster Folded cascode amplifier, a common mode feedback is needed as the high impedance node of the circuit are not set with a definite voltage bias. For the main OTA the switching common mode feed back applied easily. The gain boosters use switching common mode feedback too, with this difference that the common mode feedback capacitors work as compensation capacitor of the loop too so there is no need to extra capacitor for compensation. Schematic of the switching common mode feed back is shown in Fig 5.

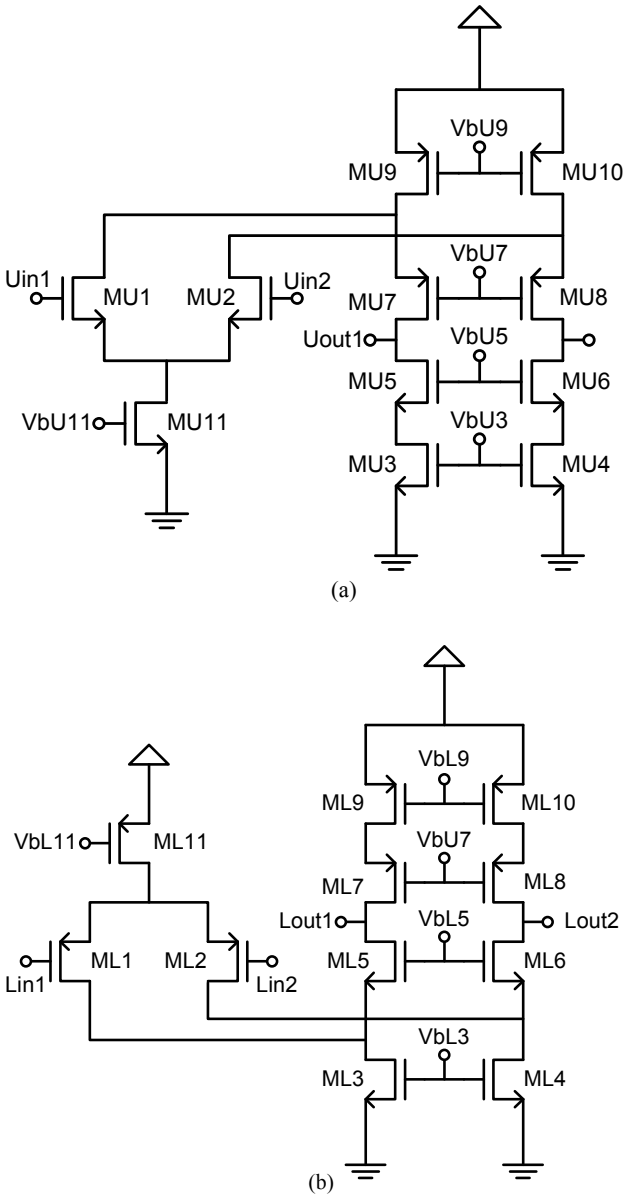

Fig. 3. Schematic of folded cascode (a) p-booster and (b) n-booster amplifier.

IV. SAMPLE-AND-HOLD AND OTHER STAGES

A. Sample-And-Hold circuit

For the sample and hold circuit a simple Flip Around topology whit bottom plate sampling is used. Schematic of a Flip Around sample-and-hold circuit is shown in the Fig. 6. Using a single capacitor as both sampling and feedback capacitor the total capacitor area is reduced in this topology. So a 4 pF capacitor is used as calculated in section II. A load of 2 pF is considered too at the out put nodes, in design state, instead of loading effect of the next stage, which is the first

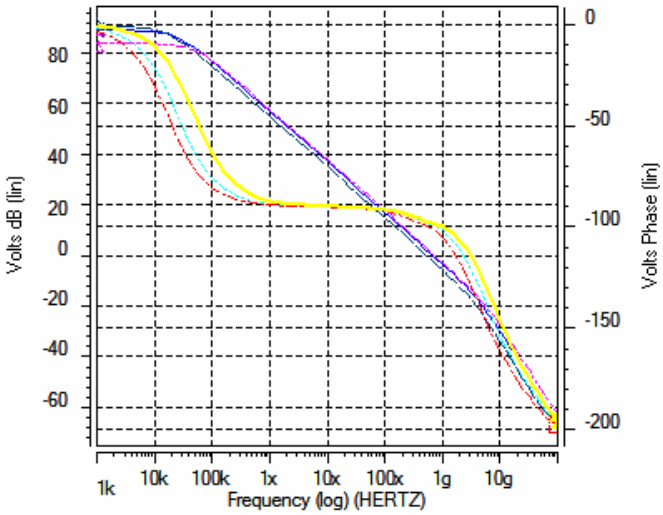

Fig. 4. The frequency response of main boosted telescopic cascode amplifier.

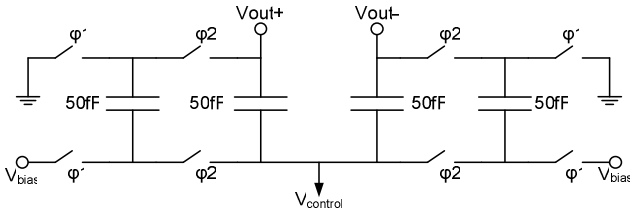

Fig. 5. Schematic of the switching common mode feed back.

TABLE III
SIZE OF DEVICES AND CAPACITORS IN SAMPLE-AND-HOLD CIRCUITS

Part Name	Device Name	Size (W/L)		
Design Number		I	II	III
Main OTA	M_1,M_2	137/.35	50/.35	80/.35
	M_3,M_4	30/.35	44/.35	87/.35
	M_5,M_6	48/.35	96/.35	192/.35
	M_7,M_8	50/.35	96/.35	199/.35
	M_9	100/.35	190/.35	399/.35
Gain booster N	M_{L1},M_{L2}	17.5/.35	35/.35	70/.35
	M_{L3},M_{L4}	9/.35	18/.35	36/.35
	M_{L5},M_{L6}	9/.35	18/.35	36/.35
	M_{L7},M_{L8}	18/.35	37/.35	74/.35
	M_{L9},M_{L10}	18/.35	37/.35	74/.35
	M_{L11}	18/.35	37/.35	74/.35
Gain Booster P	M_{U1},M_{U2}	4.5/.35	9/.35	18/.35
	M_{U3},M_{U4}	2/.35	4/.35	8/.35
	M_{U5},M_{U6}	2.5/.35	5/.35	10/.35
	M_{U7},M_{U8}	15.5/.35	31/.35	62/.35
	M_{U9},M_{U10}	10.5/.35	21/.35	42/.35
	M_{L11}	10/.35	20/.35	40/.35
$C_{sample-and-hold}$		4 pF		
C_{load}		2 PF		
$C_{Loop\_comensation}$		0.1 pF		

TABLE IV
PERFORMANCE SUMMARY OF SAMPLE AND HOLDS

Block Name	Parameter	Design Number	TT-25°	SS-90°	FF-0°
SHA	SNDR (dB)	I	91.8	92.7	97.3
		II	94	96	94
		III	86	84	88
	POWER (mW)	I	6.4	6.6	6.2
		II	10.4	10.9	10
		III	20.4	20.5	19

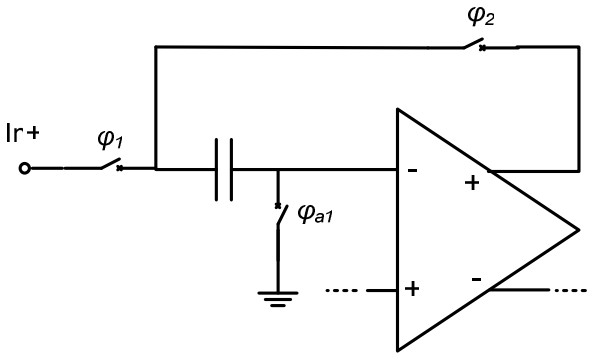

Fig. 6. Schematic of the Flip Around sample-and-hold.

residue stage. Three opamps with different bias current and slew rate is designed in the power optimizing process. The sizes of the devices in these three sample-and-hold opamp are coming in TABLE III. Summary of the calculated performance of these three designs are coming in TABLE IV. The reported result is for ideal switches as the real transmission gate switches show large nonlinearity with input variation.

B. Residue Stages

Fig. 7 (a) shows characteristic of a 2.5 bit/stage residue stage. In order to realize the characteristic, the topology, which shown in Fig. 7 (b), is utilized. Using six comparators, as a MDAC, and few logic circuits, the control bits could be generated to change voltage of the top plate of the sampling capacitors in hold mode, dependent on different input voltage levels. The characteristic and the topology schematic of the 1.5 bit/stage residue stage are shown in Fig. 8. The only difference is in the feedback gain and the number of transitions. The simulation results for performing these characteristics are shown in Fig. 9 for (a) 1.5 bit/stage and (b) 2.5 bit/stage.

In order to have some proper stage to design a high performance pipelined ADC different type of residue stage is designed for residue stage as like as sample-and-hold. Two type of design performed for 2.5 bit/stage and six for 1.5 bit/stage, three of them are introduced and will be used here. Similar to the sample-and-holds the only difference in different version of stages is in size of devices and power consumption as like as SNDR. The size of devices and capacitors, used in two different 2.5 bit/stage, are coming in TABLE V, and a

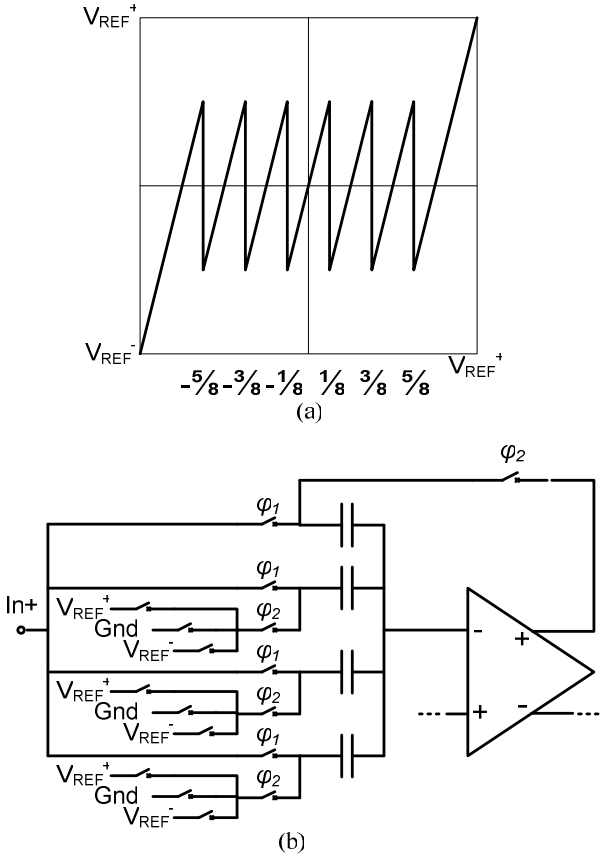

Fig. 7. (a) characteristic of a 2.5 bit/stage residue stage and (b) its circuit realization.

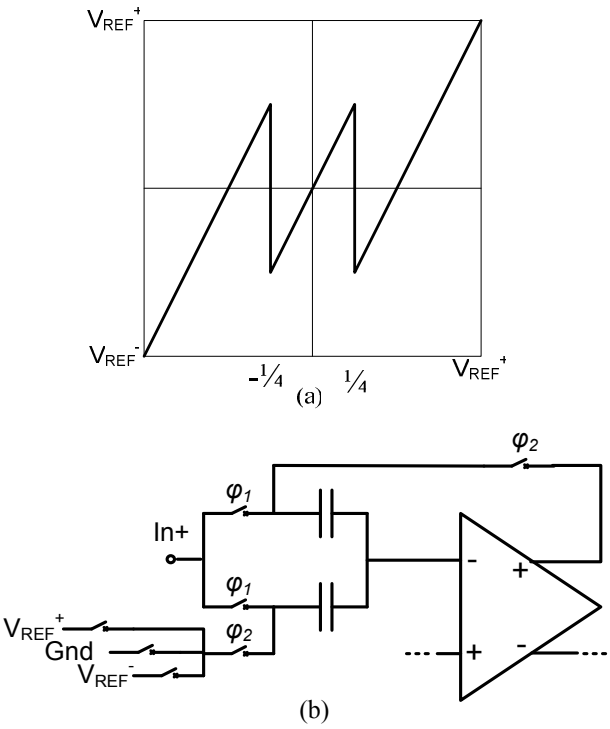

Fig. 8. (a) characteristic of a 1.5 bit/stage residue stage and (b) its circuit realization.

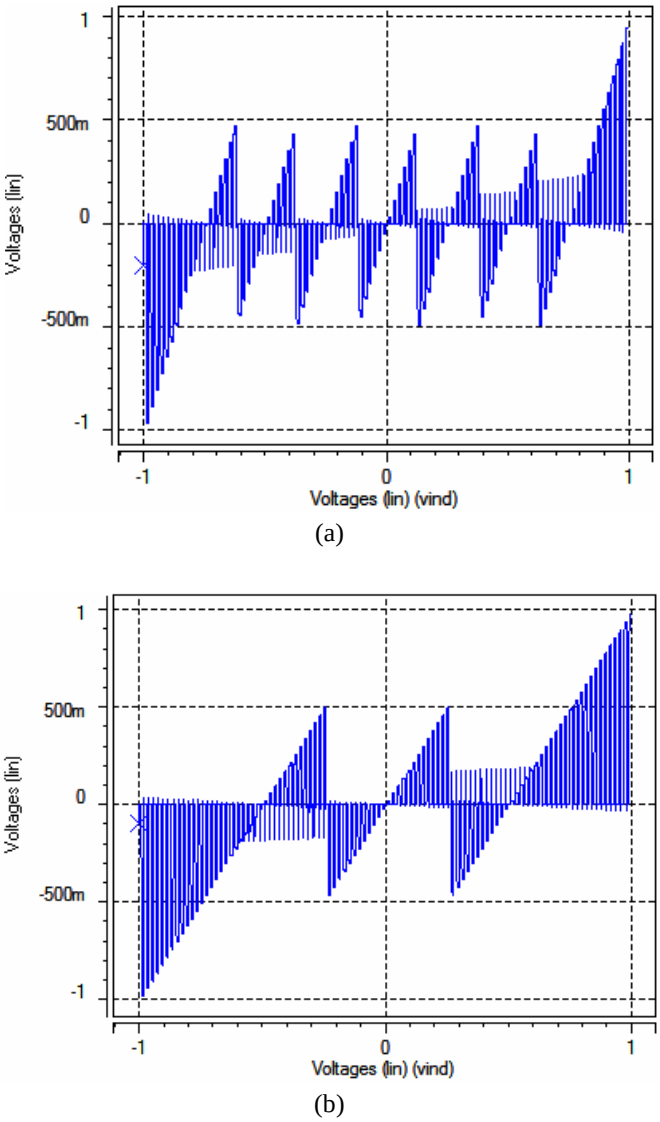

Fig. 9. Output characteristic of (a) 1.5 bit/stage and (b) 2.5 bit/stage

similar one are coming in TABLE VI for 1.5 bit /stages. The performance summary of these stages are calculated through simulation and coming in TABLE VII.

C. *Comparators and Flash Stage*

For the last two bit a three comparator flash ADC is selected. The Cho comparator is used in this design for both simplicity and less power consumption as it consumes power in half a cycle. The schematic of this comparator is shown in Fig. 10. With the minimum size of about W/L=3 each comparator consumes less than 10 µW which result in total 0.25 mw for all the comparators used in the ADC.

TABLE V SIZE OF DEVICES AND CAPACITORS IN 1.5 BIT/STAEG RESIDUE STAGES			
Part Name	Device Name	Size (W/L)	
Design Number		I	II
Main OTA	M_1,M_2	68/.35	80/.35
	M_3,M_4	42/.35	88/.35
	M_5,M_6	84/.35	192/.35
	M_7,M_8	100/.35	200/.35
	M_9	200/.35	400/.35
Gain booster N	M_{L1},M_{L2}	35/.35	70/.35
	M_{L3},M_{L4}	18/.35	36/.35
	M_{L5},M_{L6}	18/.35	36/.35
	M_{L7},M_{L8}	37/.35	74/.35
	M_{L9},M_{L10}	37/.35	74/.35
	M_{L11}	37/.35	74/.35
Gain Booster P	M_{U1},M_{U2}	9/.35	18/.35
	M_{U3},M_{U4}	4/.35	8/.35
	M_{U5},M_{U6}	5/.35	10/.35
	M_{U7},M_{U8}	31/.35	62/.35
	M_{U9},M_{U10}	21/.35	42/.35
	M_{L11}	20/.35	40/.35
$C_{sampling}$		4x0.5 pF	
C_{load}		0.5 PF	
$C_{Loop\_comensation}$		0.1 pF	

TABLE VI SIZE OF DEVICES AND CAPACITORS IN 1.5 BIT/STAEG RESIDUE STAGES				
Part Name	Device Name	Size (W/L)		
Design Number		I	II	III
Main OTA	M_1,M_2	32/.35	80/.35	70/.35
	M_3,M_4	11/.35	87/.35	35/.35
	M_5,M_6	24/.35	13/.35	35/.35
	M_7,M_8	25/.35	13/.35	18/.35
	M_9	50/.35	26/.35	35/.35
Gain booster N	M_{L1},M_{L2}	9/.35	5/.35	-
	M_{L3},M_{L4}	4.5/.35	2.5/.35	-
	M_{L5},M_{L6}	4.5/.35	2.5/.35	-
	M_{L7},M_{L8}	9/.35	5/.35	-
	M_{L9},M_{L10}	9/.35	5/.35	-
	M_{L11}	9/.35	5/.35	-
Gain Booster P	M_{U1},M_{U2}	2.5/.35	2.5/.35	-
	M_{U3},M_{U4}	1.5/.35	.7/.35	-
	M_{U5},M_{U6}	2/.35	.7/.35	-
	M_{U7},M_{U8}	8/.35	4/.35	-
	M_{U9},M_{U10}	5.5/.35	3/.35	-
	M_{L11}	5/.35	3/.35	-
$C_{sampling}$		4x0.25 pF		
C_{load}		0.5p PF		
$C_{Loop\_comensation}$		0.1 pF		-

TABLE VII PERFORMANCE SUMMARY OF RESIDUE STAGES					
Block Name	Parameter	Design Number	TT-25˚	SS-90˚	FF-0˚
2.5 bit/stage	SNDR (dB)	I	81.9	78.9	79.1
		II	80.6	82.5	82.5
	POWER (mW)	I	11.7	11.7	11.7
		II	21.1	21.7	21
1.5 bit/stage	SNDR (dB)	I	71.8	71.5	72.6
		II	68.6	68.2	67.6
		III	60	54.7	55.3
	POWER (mW)	I	3.7	3.8	3.7
		II	2.4	2.4	2.4
		III	1.1	1.1	1.1

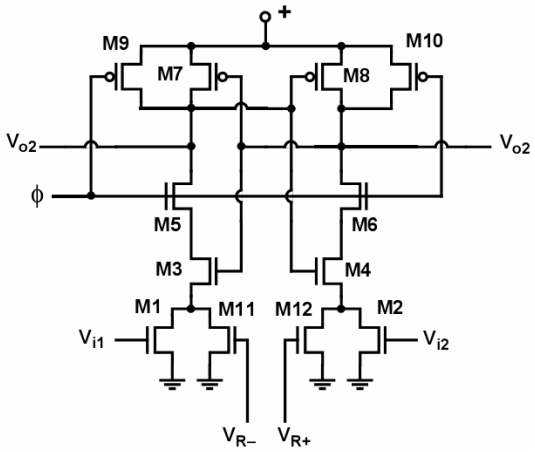

Fig. 10. The schematic of the cho comparator

TABLE VIII PERFORMANCE SUMMARY OF FULL ADC				
Block Name	Stage type	Power Consumption (mW)		
		TT-25˚	SS-90˚	FF-0˚
SHA	SHA II	10.4	10.9	10
1st RS	2.5 bit/stage I	11.7	11.7	11.7
2nd RS	1.5 bit/stage I	3.7	3.8	3.7
3rd RS	1.5 bit/stage II	2.4	2.4	2.4
4th RS	1.5 bit/stage II	2.4	2.4	2.4
5th RS	1.5 bit/stage II	2.4	2.4	2.4
6th RS	1.5 bit/stage III	1.1	1.1	1.1
7th RS	1.5 bit/stage III	1.1	1.1	1.1
8th RS	1.5 bit/stage III	1.1	1.1	1.1
9th RS	1.5 bit/stage III	1.1	1.1	1.1
Flash	2 bit Cho comp.	0.03	0.03	0.03
Total Pipelined ADC		**37.4**	**38.0**	**37.0**

V. PIPELINED ADC

As it is mentioned in pipeline structure section the pipelined ADC requirements guide us to select the stages. At first step the requirements of the TABLE I considered and the full pipelined ADS performed. Another consideration with similar linearity stages was power consumption. In this case the lower power consumption obviously give priority to use. In order to have correct full range quantization in the ADC a step of full range is applied to the input and the output bits where followed to show the full range. Due to some unconsidered non idealities, such as input capacitance of the loading stage, the full range wasn't shown at out put bit and so a better linearity for each stage considered. The final arrangement of the pipelined stage is coming in TABLE VIII in addition to the total power consumption.

The design of the full pipeline ADC is under process of doing and the whole ADC performance will be reported in future.

How we can reduce this power up to half of this?

The idea of power reducing power consumption in this architecture is opamp reuse. The opamps are the most power consuming components in this ADC architecture. opamps are used in one phase of clock which is half a period. In other phase the opamp is Idle with both inputs and outpout connected to ground. As two following stage has reverse phase of opamp using and as the clock phases are non-overlapping we may can borrow the opamp of each stage from the preceding stage. The main problem is that the opamps may differ from one stage to another in both linearity and timing performance. This problem could be solved using proper dividing factor for capacitors as done in this work, at least equal for two following stage and using more accurate opamp for the next stage. As the opamp of the sample-and-hold characteristics is similar to the first residue stage's opamp, if we share one opamp for both of them and do this up to last stages two by two the power will be reduces up to half of its current value. It means that, a low power, 20 mW, high speed opamp could be designed in the case of opamp reuse. Additionally this technique will reduce the area by factor of about two which further make design suitable to be embeded in today's and future high performance systems.

CONCLUSION

Different blocks for a 38mW 12bit 100MS/s pipelined ADC has been designed. Using wide swing folded cascode gain boosters a high linear fast speed OTA has peen introduced. A technique has been proposed to lowering the power consumption up to abouts 20 mW.

REFERENCES

[1] V. Gopinathan, ISSCC, Session 12, Nyquist ADCs, Overview, Jan 2006.

[2] N. Verma, A. P. Chandrakasan, "A 25µW 100kS/s 12b ADC for WirelessMicro Sensor Applications", ISSCC, Jan 2006.

[3] G. Geelen, et. Al., "A 90nm CMOS 1.2V 10b Power and Speed Programmable Pipelined ADC with 0.5pJ/Conversion-Step," ISSCC, Jan 2006.

[4] S. T. Ryu, et. Al., "A 10b 50MS/s Pipelined ADC with," ISSCC, Jan 2006.

[5] P. Bogner, et. Al., "A 14b 100MS/s Digitally Self-Calibrated Pipelined ADC in 0.13µm CM," ISSCC, Jan 2006.

[6] T. Sepke, et. Al., "Comparator-Based Switched-Capacitor Circuits For Scaled CMOS Technologies," ISSCC, Jan 2006.

[7] B.Razavi, RF Microelectronics. PRENTICE HALL PTR, ch.2, pp.45, 1998.

[8] K. Bult, et. Al. "A Fast-Setteling Cmos Op Amp for SC Circuits with 90-dB DC Gain", IEEE Journal of Solid-State Circuits, vol. 25, No. 6, Dec. 1990.