

## Electronics III

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**Class Hours:** Sat.-Mon. 9:30-11:00  
**Teacher Assistants:**

## Course Outline

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### *Models for Integrated-Circuit Active Devices*

## Course Outline

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- **MOS Transistor Models and physics**
- MOSFET and Junction FET
- MOS capacitor
- MOS threshold
- MOS regions (linear & saturation ) characteristic
- Small-Signal Model
- Examples of small-signal Analysis
  - Transconductance Amp
  - Diode
  - Source Follower
- Capacitance
- Higher order models

**References:**  
**Razavi's IC Book, L&S**

## Course Outline

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- **Bipolar Transistor Models**
- Hybrid-small-signal model (for BJT)
  - model elements
    - Common-Emitter (current drive, voltage drive )
    - Common-Collector
    - Common - Base
    - Ohmic Resistance
- Lateral PNP transistors
- Other Components
  - Base diffusion resistor
  - Other resistor
  - Capacitor
  - Inductor

**References:**  
**Gray & Mayer's IC Book, L&S**

## Course Outline

- **Single- Stage Amplifiers**
- *Basic Concepts*
- *Common-Source Stage*
  - Common-Source Stage with Resistive Load
  - CS Stage with Diode-Connected Load
  - CS Stage with Current-Source Load
  - CS Stage with Triode Load
  - CS Stage with Source Degeneration
- *Source follower*
- *Common-Gate Stage*
- *Cascode stage*
  - Folded Cascode
- *Choice of Device Models*

**Reference:  
Razavi's IC Book**

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## Course Outline

- **Differential Amplifiers**
- *Single-Ended and Differential operation*
- *Basic Differential Pair*
  - Qualitative Analysis
  - Quantitative Analysis
- *Common mode Response*
- *Differential Pair with MOS Loads*
- *Gilbert Cell*

**Reference:  
Razavi's IC Book**

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## Course Outline

- **Frequency Response of Integrated circuits**
- *Single-Stage Amplifier frequency response*
  - Differential Amp frequency response
  - Common-Mode (CM) gain in diff pair
  - Emitter-follower freq response
  - Common-Base freq response
- *multistage Amp freq response*
  - Dominant Pole Approximation
  - Zero-value Time constant Analysis
  - Common-Emitter cascode freq response
  - Cascode freq response

**References:  
Razavi,  
Gray & Mayer's  
IC Book**

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## Course Outline

- **Elementary Transistor stages**
- *MOS single Transistor Amplifying stages*
  - Biasing ,Gain ,Bandwidth , high frequency performance ,
  - Unity- Gain freq & GBW product
- *Source & Emitter Followers*
  - DC level shift ,high freq Gain ,Output Impedance
- *Cascode Transistors*
  - MOS cascode (Low freq Analysis ,high freq performance).
  - Bipolar cascode
- *Cascode stages*
  - BW of cascode w/ low and w/Active load ,High voltage cascode,
  - cascode w/Bipolar ,Feedforward in cascode Amp

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## Course Outline

- **Differential Stage**  
*MOS differential stages (DC characteristic , small-signal behavior ,low freq analysis ,GBW product, Slew-rate)*
- **Current mirrors**  
*Simple MOS current Mirror*  
*Other current mirror*  
*Bipolar current mirror*  
*Gain factor mismatch*  
*Body factor mismatch*  
*Offset voltage*  
*Mismatch effects on Current mirror*  
*Differential stage w/ Active load*  
*CMRR*  
*Design for low offset and drift*  
*Power Supply Rejection Ratio (PSRR)*

## Course Outline

- **Design options :**  
*Design for optimum GBW or SR*  
*Compensation of the Positive Zero*

**Reference: L&S**

## Course Outline

- **Frequency Response stability of feedback Amplifiers**
- **The Stability Problem**

**References:**  
**Gray & Mayer IC book,**  
**Sedra & Smith**

## Course Outline

- **Operational Amplifier Design**
- **Design of a simple CMOS OTA**  
*Gain*  
*GBW and  $\Phi_M$*
- **Design plan : optimization for Maximum GBW**
- **The Miller CMOS OTA**  
*Operation*  
*Gain*  
*GBW and  $\Phi_M$*   
*Design plan : Determine Compensation Cap Cc Determine size and I*

## Course Outline

- Full set of characteristic of Miller OTA
  - CM input vs. supply
  - Output voltage range vs. Supply
  - Max output current (sink and source)
  - AC analysis :low freq.
  - GBW vs..  $I_{BIAS}$
  - Slew-rate vs. load cap
  - Output voltage range vs. Frequency
  - Settling time
  - Output Impedance
  - temperature effects
- Matching characteristics
  - transistor Mismatch model
  - Threshold voltage Mismatch  $V_T$

**Reference:  
L&S**

## Course Outline

- **And Special Issues**

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## References

- **Design of Analog CMOS Integrated Circuit**, Behzad Razavi  
McGraw-Hill 2001
- **Analysis and design of Analog Integrated Circuits**, Gray –  
Hurst-Lewis- Mayer Forth Edition John Wiley & SONS,INC 2004
- **Design of Analog Integrated circuit & systems**, Kenneth R.  
Laker, Willy M.C .Sansen .McGraw-Hill 1994
- **Microelectronic Circuit**, Adel S. Sedra , Kenneth C. Smith ,  
Saunders College publishing 1991
- **Analog Integrated Circuit Design** ,David A. Johns ,Ken Martin  
,John Wiley & Sons ,Inc,1997

## Grading

**Assignment : 10%**

**Project : 20%**

**Quiz :10%**

**Mid term :20%**

**Final term :40%**

## Field Effect Transistors (FET)

**JFET:** Junction FET

**MOSFET(MOST):** Metal-Oxide Semiconductor FET

**Fig 1.1 a**  
n-channel JFET

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## Field Effect Transistors (FET)

- Channel is sandwiched between two depletion layers which isolate channel from two conducting layer: Gate ( $p+$  in  $n$ -channel) and substrate ( $p$  in  $n$ -channel).
- These depletion layers form junction capacitances between the channel to the top gate  $C_{gs}$  and to the bottom layer  $C_{bc}$ . The voltage across each capacitance controls the widths of the depletion layer and hence, the widths of the residual channel between both depletion layers. The voltage across  $C_{gs}$  and  $C_{bc}$  control the conductivity of the channel as well as its charge, so, the current. Either  $C_{gs}$  or  $C_{bc}$  can independently control the current through channel.

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## Field Effect Transistors (FET)

**Fig 1.1 b**  
p-channel JFET

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## Field Effect Transistors (FET)

- The channel is isolated from the top gate  $G$ , by a depletion layer with width  $h$ . The channel is also isolated from the substrate or bulk  $B$ , by another depletion layer.
- Both depletion layers modulate the channel conductivity or pinch-off (no  $I_D$  current,  $I_D = 0$  the channel entirely).
- This (pinch-off) can be done by reverse biasing the voltage across these depletion layers (respect to the source).
- Note usually the bulk is at a constant negative voltage or connected to source so only the top gate (like CMOS) is used to control the transistor current.
- The depletion layer of the top gate  $G$  can fully pinch off the channel, provided its thickness  $h$  is made equal to the thickness of the channel  $a_c$ .
- The voltage  $V_{GS}$  requested to fully pinch-off the channel (for zero  $V_{DS}$ ) is called pinch-off voltage  $V_P$ .

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## Field Effect Transistors (FET)

Consider a PN Junction (Fig 1.2)

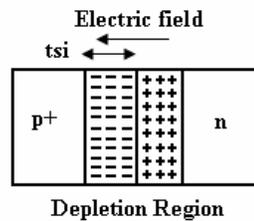


Fig 1.2  
PN Junction

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## Field Effect Transistors (FET)

- In the **p+** side a large number of free positive carriers are available, whereas in the **n** side, many free negative carriers are available.
- The hole, in the **p+** side tend to diffuse in to the **n** side, whereas the free electrons in the **n** side tend to diffuse to the **p+** side.
- This diffusion lowers the concentration of free carriers in the region between the two sides.
- As the two types of carriers diffuse together, they recombine. Every electron that diffuse from n-side to the p-side leaves behind a “**bound**” positive charge close to the transition region. Similarly, every hole that diffuse from the p-side leaves behind a bound electron near transition region.
- This diffusion of free carriers create a depletion region at the junction of the two sides where no free carriers exist.

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## Field Effect Transistors (FET)

- The total amount of “bound” charge on the two sides of junction must be equal for charge neutrality.
- This requirement causes the depletion region to extend further into the more lightly doped n-side than into the p+ side.
- As these bound charges are exposed, an electric field develops going from the n-side to the p-side. This electric field is often called the built-in potential of the junction. It opposes the diffusion of free carriers until there is no movement of charge under open-circuit condition.

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## Field Effect Transistors (FET)

Recall for a one-sided abrupt junction, the thickness of the depletion layer is:

$$t_{si} = \sqrt{\frac{2\epsilon_{si}(\Phi_j - V_{BC})}{qN_{SUB}}} \text{ or } (\Phi_j + V_R) \quad \text{Where } V_R = -V_{Bis} \text{ is the reverse bias voltage across p-n junction} \quad (1-1)$$

The layer reverse bias is the thicker depletion layer becomes

$V_{BC}$  is the reverse bias voltage

$\Phi_j$  is the bulk-channel junction built-in voltage

$$\Phi_j = \frac{kT}{q} \ln \frac{N_c N_{SUB}}{n_i^2} \quad n_i = 1.5 \times 10^{10} / \text{cm}^3 @ 27^\circ\text{c} \quad (1-2)$$

Note that always  $V_{SB} > 0$  for nmos

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## Field Effect Transistors (FET)

Substituting  $V_{BC}$  by  $V_p$  and  $t_{si}$  by  $a_c$ :

$$V_p = \frac{qN_A a_c^2}{2\epsilon_{si}} - \Phi_j \quad \text{doping in p+ in channel} \quad (1-3)$$

This JFET is depletion type, meaning the conducting channel already exists for  $V_{GS} = 0$  must be positive.

By means of Ion-implantation technology, thinner channels ( $< 0.2 \mu\text{m}$ ) can be realized

$$V_p = 1V \rightarrow a_c \approx 0.16 \mu\text{m}$$

$$V_p = 0V \rightarrow a_c \approx 0.11 \mu\text{m}$$

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## Field Effect Transistors (FET)

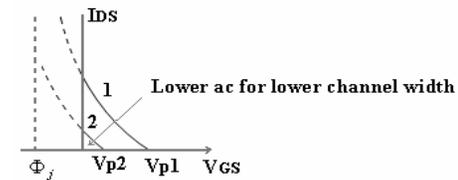


Fig 1.3

The forward bias  $V_{GS}$  are shown by dashed lines in Fig 1.3. Higher than the diode voltage large forward current starts to flow through gate. Forward bias gate must be avoided due to gate leakage current.

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## MOST

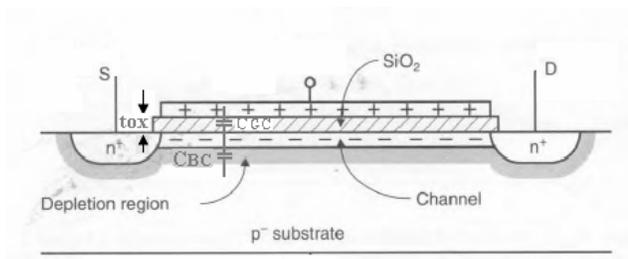


Fig 1.4 a  
nMOST

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## MOST

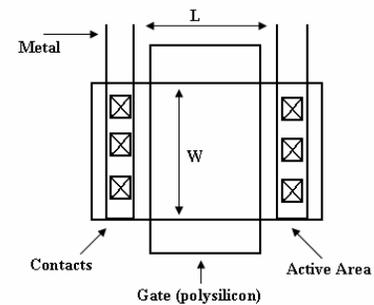


Fig 1.4 b  
nMOST layout

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## MOST

- Channel is sandwiched between an oxide layer and a depletion layer. These oxide and depletion layers isolate channel from two conductive layers (Gate) and (Substrate).
- These isolation layers again form caps:  $C_{GC}$  and  $C_{BC}$
- $C_{GC}$  is an oxide cap but  $C_{BC}$  is a depletion cap.
- Oxide cap is less efficient:

$$\epsilon_{ox} = 0.34 \text{ pF/Cm} \quad \epsilon_{si} = 1.06 \text{ pF/Cm}$$

$$\Rightarrow \epsilon_{si} \approx 3\epsilon_{ox}$$

## MOST

- Oxide cap is independent of the applied voltage!
- The applied voltage on  $C_{GC}$  and  $C_{BC}$  control the charge in residual channel and so the current.
- Current establishes if  $V_{GS} > V_{th}$  (threshold voltage) for  $V_{DS} > 0$

## MOST

- pmos and nmos need substrate material of opposite type

Fig 1.5  
N-well CMOS technology

## MOS Capacitance (Oxide)

$$C_{GC} = WLC_{ox} \quad C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \quad (1-4)$$

Examples:

For 0.25  $\mu\text{m}$  technology  $t_{ox} = 4\text{nm} = 40 \text{ \AA}$

$C_{ox} = 8.5 \text{ fF}/\mu\text{m}^2$  Very efficient capacitance

Very old technology  $t_{ox} = 50\text{nm}$   $C_{ox} = 6.8 \times 10^{-8} \text{ F/Cm}^2 = 0.68 \text{ fF}/\mu\text{m}^2$   
 $WL = (50 \times 5) \mu\text{m}^2 \Rightarrow C_{GC} = 0.17 \text{ pF} = 170 \text{ fF}$

For modern technologies:  $C_{GC} = 2.125 \text{ pF} (WL = 250 \mu\text{m}^2)$

## MOS Capacitance (Junction)

$$C_{BC} = WLC_j \quad C_j = \frac{\epsilon_{si}}{t_{si}} \quad (1-5)$$

Where  $t_{si}$  is the thickness of depletion layer between channel and bulk.  $t_{si}$  depends on the voltage across the depletion layer and on the doping level  $N_{SUB}$  of the substrate.

For an abrupt junction:

$$t_{si} = \sqrt{\frac{2\epsilon_{si}(\Phi_j - V_{BC})}{qN_{SUB}}} \quad \Phi_j = \frac{kT}{q} \ln \frac{N_c N_{SUB}}{n_i^2}$$

$$n_i = 1.5 \times 10^{10} / \text{cm}^3 @ 27^\circ\text{C}$$

$\Phi_j$  is the reverse bias voltage (some times referred to as  $\Phi_0$ )  
 $V_{BC}$  is the bulk-channel junction built-in voltage

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## MOS Capacitance (Junction)

Normally  $V_{BC} = V_{BS}$  (channel and source potential the same at the source side)

**Note:** As  $\Phi_F = \frac{kT}{q} \ln \frac{N_{SUB}}{n_i}$  if  $N_C = N_{SUB} \Rightarrow \Phi_j = 2\Phi_F$

**Note:**  $V_R \uparrow \Rightarrow t_{si} \uparrow \Rightarrow C_j \downarrow$

**Note:**  $\Phi_j - V_{BC} = \Phi_j - V_B + V_{ch} \Rightarrow$

For  $V_{ch} = V_D$  since  $V_D > V_S$  (as in nmos p-sub is grounded so is more reverse biased) so  $t_{si}$  is thicker in Drain side!

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## MOS Capacitance (Junction)

for  $N_{SUB} = 3 \times 10^{14} \text{ cm}^{-3}$   $n^+, N_C = 2 \times 10^{17} \text{ cm}^{-3}$ :

$$\Phi_j = 0.68\text{V} \quad \text{Almost 1/10 of } C_{ox}$$

for  $V_{BS} = 0 : t_{si} = 1.73 \mu\text{m} \Rightarrow \left\{ \begin{array}{l} C_j = 0.67 \times 10^{-8} \text{ F/cm}^2 \\ C_{BC} = 15 \text{ fF} \end{array} \right\}$

Note: The depletion layer thickness (1730 nm)  $\gg$  Oxide thickness (50nm) so always:

$$C_{BC} \ll C_{GC}$$

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## Model MOST-JFET

- MOST is actually a parallel connection of a MOST and a JFET (parasitic) which is usually common for all MOST (single substrate). note that JFET is always off
- Gate control is seen as a MOST (CMOS) and the bulk control is regarded by JFET in this model!
- The effect of parasitic JFET in a MOST is shown in  $\gamma$  value by  $\gamma$  (gamma) factor. This is so called body factor.

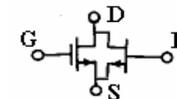


Fig 1.6  
MOSFET-JFET Model

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## Model MOST-JFET

$$\gamma = \frac{\sqrt{2\epsilon_{si}qN_{SUB}}}{C_{ox}} \quad V^{1/2} \text{ dimension} \quad (1-6)$$

By one of the expressions of  $C_{BC}$  and  $C_{GC}$  we can write:

$$\left\{ \begin{array}{l} C_{BC} = WLC_j = WL \frac{\epsilon_{si}}{\sqrt{\frac{2\epsilon_{si}(\Phi_j - V_{BS})}{qN_{SUB}}}} = WL \frac{\sqrt{\epsilon_{si}qN_{SUB}}}{\sqrt{2(\Phi_j - V_{BS})}} \\ C_{GC} = WLC_{ox} \end{array} \right.$$

$$\Rightarrow \frac{C_{BC}}{C_{GC}} = \frac{\sqrt{\epsilon_{si}qN_{SUB}}}{C_{ox}} \cdot \frac{1}{\sqrt{2(\Phi_j - V_{BS})}} = \frac{\sqrt{2\epsilon_{si}qN_{SUB}}}{C_{ox}} \cdot \frac{1}{2\sqrt{(\Phi_j - V_{BS})}}$$

$$\Rightarrow \gamma = \frac{C_{BC}}{C_{GC}} 2\sqrt{\Phi_j - V_{BS}} = \frac{C_{BC}}{C_{GC}} 2\sqrt{\Phi_j + V_{SB}} \quad (1-7)$$

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## Model MOST-JFET

- The depletion charge  $Q_D$  contributing to threshold voltage is function of  $V_{BS}$ . This charge depends on the depletion thickness  $t_{si}$  as given by  $Q_D = qN_{Bulk}t_{si}$  so:

$$\frac{Q_D}{C_{ox}} = \frac{qN_{Bulk}}{C_{ox}} \sqrt{\frac{2\epsilon_{si}(\Phi_j - V_{BS})}{qN_{Bulk}}} \leftarrow t_{si} \quad (1-8)$$

$$\therefore \frac{Q_D}{C_{ox}} = \frac{\sqrt{2qN_{Bulk}\epsilon_{si}}}{C_{ox}} \sqrt{2|\Phi_F| - V_{BS}} \quad * \quad (1-9)$$

- The minimum voltage needed on surface to push down the depletion region is  $\Phi_j = 2|\Phi_F|$  or the voltage to just create mobile electrons (charges).

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## Model MOST-JFET

- equation(\*) for 1)  $V_{BS} = 0$   $\frac{Q_D}{C_{ox}} = \gamma\sqrt{2|\Phi_F|}$   
2)  $V_{BS} < 0$   $\frac{Q_D}{C_{ox}} = \gamma\sqrt{2|\Phi_F| - V_{BS}}$

so defining  $V_{T0}$  for  $V_T$  when  $V_{BS} = 0$  is obvious that  $V_T$  is greater than  $V_{T0}$  for  $V_{BS} < 0$  as follows:

$$V_T = V_{T0} + \gamma(\sqrt{2|\Phi_F| - V_{BS}} - \sqrt{2|\Phi_F|}) \quad (1-10)$$

- In other words, say in NMOS, when  $V_{BS} < 0$  source/channel voltage is higher respect to bulk there are positive charges on the top plate of  $C_{CB}$  (due to charge in depletion region). therefore in order to cancel these extra charges the more positive voltage than  $V_{T0}$  must be applied on top plate of  $C_{CB}$  that it's bottom plate (i.e. channel) produces more negative charges to account for depleted positive charges on the surface.

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## Model MOST-JFET

- So body factor  $\gamma$  is directly proportional to the ratio of controlling caps  $C_{BC}$  and  $C_{GC}$ . The proportionality factor  $\frac{C_{BC}}{C_{GC}}$  is the voltage dependence of the bulk junction capacitance  $C_{BC}$ .

**A Definition:**

$$n - 1 = \frac{C_{BC}}{C_{GC}} = \frac{\gamma}{2\sqrt{\Phi_j - V_{BS}}} > 0 \quad (1-11)$$

- Note:  $n$  depends on the applied voltage  $V_{BS}$  whereas  $\gamma$  does not. Parameters  $\gamma$  and  $n$  are the first two parameters of the MOST model that depends on  $N_{SUB}$  and  $\epsilon_{si}$  values.

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## Model MOST-JFET

Example:

For:

$$C_{ox} = 6.8 \times 10^{-8} \text{ F/cm}^2, n_{sub} = 3 \times 10^{14} \text{ cm}^{-3}$$

$$\Rightarrow \gamma = 0.15V^{1/2} \text{ for } V_{BS} = 0 \Rightarrow n = 1.09$$

But for:

$$n_{sub} = 10^{16} \text{ cm}^{-3} \Rightarrow \gamma = 0.86V^{1/2}, n = 1.49$$

**Note:** GAMMA ( $\gamma$ ) is a constant SPICE model parameter not  $n$ . it is obvious that  $n$  is bias dependent.

## MOST Threshold Voltage

$V_{T0}$  is obtained from semiconductor physics for  $V_{BS} := 0$

$$V_{T0} = \Phi_{GB} - \frac{Q_{ox}}{C_{ox}} + 2\Phi_F \pm \frac{Q_D}{C_{ox}} \quad (1-12)$$

With + for nMOST and - for pMOST. It is independent of the voltage applied.

## MOST Threshold Voltage

$V_{T0}$  terms:

1)  $\Phi_{GB}$  is the difference in the work function between the gate material and the bulk material.

With n+ polysilicon with  $\Phi_{sp}$  doping for gate: for p-bulk doping of (nMOST):  $N_B$

$$\Phi_{GB} = -\frac{kT}{q} \ln \frac{N_G N_B}{n_i^2} \quad N_B \approx [3 \times 10^{14} - 10^{16}] \text{ cm}^{-3} \quad (1-13)$$

$$N_G \approx 2 \times 10^{19} \text{ cm}^{-3}$$

for a pMOST: for n-bulk doping  $N_B$ :

$$\Phi_{GB} = -\frac{kT}{q} \ln \frac{N_G}{N_B} \quad N_B \approx [3 \times 10^{14} - 10^{16}] \text{ cm}^{-3} \quad (1-14)$$

## MOST Threshold Voltage

2) Charge  $Q_{ox}$  represents the positive charges (in  $C_{cm}$ ) at the silicon-oxide interface. New technology tries to minimize them to avoid  $dV_{th}$ . In SPICE is  $Q_{ox}$  represents by NSS.

Flat Band Voltage:

$$V_{FB} = \Phi_{GB} - \frac{Q_{ox}}{C_{ox}} \quad (1-15)$$

It is the gate-source potential that causes no band bending in the silicon.

## MOST Threshold Voltage

- 3) The surface potential at the source side of the channel under strong inversion is  $2\Phi_F$  (PHI in SPICE). Its value is obtained from the distance between the Fermi level (in the bulk) and the middle of the energy bandgap of the semiconductor material. It also represents the band bending in strong inversion:

$$\Phi_F = \pm \frac{kT}{q} \ln \frac{N_{sub}}{n_i} \quad (1-16)$$

+ for nMOST and - for pMOST.  
So  $\Phi_F$  is a measure of the doping level, as well as conductivity.

## MOST Threshold Voltage

- 4) The depletion charge  $Q_D$  which depends on the depletion layer thickness  $t_{si}$

$$Q_D = qN_B t_{si} \Rightarrow \pm \frac{Q_D}{C_{ox}} = \pm \frac{qN_B}{C_{ox}} \sqrt{\frac{2\epsilon_{si}(\Phi_j - V_{BS})}{qN_B}} = \pm \frac{\sqrt{2\epsilon_{si}qN_B(\Phi_j - V_{BS})}}{C_{ox}} \quad (1-17)$$

$$\therefore \pm \frac{Q_D}{C_{ox}} = \pm \gamma \sqrt{(\Phi_j - V_{BS})} \cong \pm \gamma \sqrt{2|\Phi_F|} \quad \text{Note: built-in junction potential}$$

for ( $V_{BS} = 0$ )  $\Phi_j \cong 2|\Phi_F|$

$$\Rightarrow \pm \frac{Q_D}{C_{ox}} = \pm \gamma \sqrt{2|\Phi_F| - V_{BS}} \quad (1-18)$$

Note:  $V_{BS}$  is negative such that  $V_{BS}$  and  $2|\Phi_F|$  add up!  
 $V_T$  is then as follows:

$$V_T = V_{T0} \pm \gamma (\sqrt{2|\Phi_F| \mp V_{BS}} - \sqrt{2|\Phi_F|}) \quad (1-19)$$

$\gamma$   $\mathbb{M}_T$  represents the body effect (or the effect of parasitic JFET)

## Deviation of I/V Characteristics

Consider a semiconductor bar carrying a current  $I$ . If the charge density along the direction of current is  $Q_d$  coulombs per meter and the velocity of charge is  $v$  meters per second then:

$$I = Q_d \cdot v \quad (1-20)$$

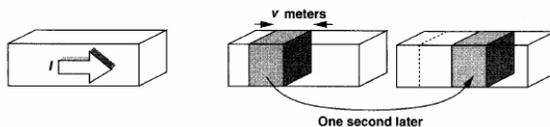


Fig 1.7  
Semiconductor bar

## Deviation of I/V Characteristics

Now consider an NFET whose source and drain are connected to ground (Fig 1.8a). The inversion charge density produced by the gate oxide cap. is proportional to  $V_{GS} - V_T$ . For  $V_{GS} \geq V_T$  any charge placed on the gate must be mirrored by the charge in the channel, yielding a uniform channel charge density equal to:

$$Q_d = WC_{ox}(V_{GS} - V_T) \quad (1-21)$$

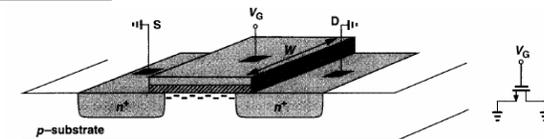


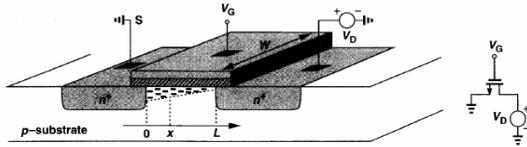
Fig 1.8a  
Channel charge (equal source and drain voltage)

## Deviation of I/V Characteristics

Now suppose that the drain voltage is greater than zero (Fig 1.8b). The local voltage difference between gate and channel varies from  $V_{GS}$  to  $V_{GS} - V_D$ . The charge density at a point  $x$  along the channel is:

$$Q_d(x) = WC_{ox}(V_{GS} - V(x) - V_T) \quad (1-22)$$

Where  $V(x)$  is the channel potential at  $x$



**Fig 1.8 b**  
Channel charge (unequal source and drain voltage)

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## Deviation of I/V Characteristics

From (1-20) the current is given by:

$$I_D = -WC_{ox}(V_{GS} - V(x) - V_T) \cdot v \quad (1-23)$$

$$v = -\mu_n \frac{dV(x)}{dx} \quad (1-24)$$

$$\Rightarrow I_D = -WC_{ox}(V_{GS} - V(x) - V_T) \mu_n \frac{dV(x)}{dx} \quad (1-25)$$

Considering the boundary conditions  $V(0) = 0; V(L) = V_{DS}$  we obtain:

$$\int_{x=0}^L I_D dx = \int_{V=0}^{V_{DS}} WC_{ox} \mu_n (V_{GS} - V(x) - V_T) dV \quad (1-26)$$

$$I_D = \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2] \quad (1-27)$$

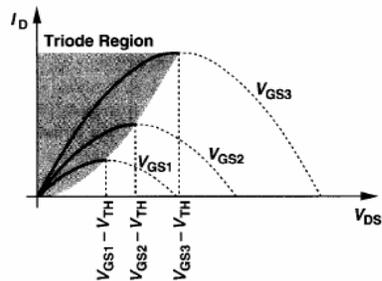
Note: L is the effective channel length

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## Deviation of I/V Characteristics

Regarding (1-27)



**Fig 1.9**  
Drain current versus Drain-source voltage  
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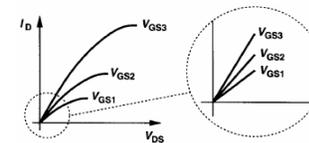
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## Deviation of I/V Characteristics

If in (1-27),  $V_{DS} \ll 2(V_{GS} - V_T)$  then:

$$I_D \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS} \quad (1-28)$$

$$\Rightarrow R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)} \quad (1-29)$$



**Fig 1.10**  
Linear operation in deep triode region  
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## Deviation of I/V Characteristics

In reality the drain current does not follow the parabolic behavior for (Fig 1.11), and becomes relatively constant (saturation region)

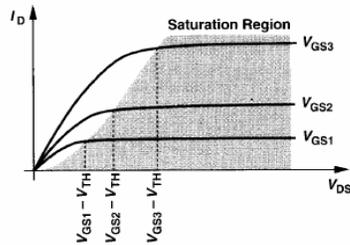


Fig 1.11

Linear operation in deep triode region

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## Deviation of I/V Characteristics

The density of inversion layer charge is proportional to  $V_{GS} - V_T$  if  $V_T$  approaches  $V_{GS}$ , then  $V_{GS} - V_T$  drops to zero (Pinch-off). As  $V_{DS}$  increases further, the point at which  $V(x) = 0$  gradually moves toward the source (Fig 1.12). Now reconsidering (1-26) with  $x = 0$  to  $x = L_{pinch-off}$  and  $V(x) = 0$   $V(x) = V_{GS} - V_T$  come to:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L_{pinch-off}} (V_{GS} - V_T)^2 \approx \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 \quad (1-30)$$

Almost independent of drain-source voltage

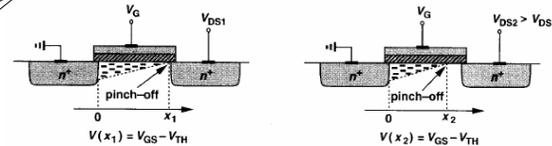


Fig 1.12

Pinch-off behavior

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## Deviation of I/V Characteristics

Since a MOSFET operating in saturation produces a current in response to its gate-source overdrive voltage, we can define **Transconductance** to define how well the device converts voltage to current. **Transconductance** is denoted by  $g_m$  and expressed as:

$$g_m = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{V_{DS}=cte} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) \quad (1-31)$$

Transconductance represents the sensitivity of the device. it can be shown that:

$$g_m = \sqrt{2 \mu_n C_{ox} \frac{W}{L} I_D} \quad (1-32)$$

$$= \frac{2 I_D}{V_{GS} - V_T} \quad (1-33)$$

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## Deviation of I/V Characteristics

Fig 1.13 shows  $g_m$  behavior

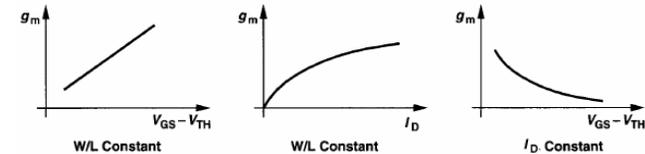


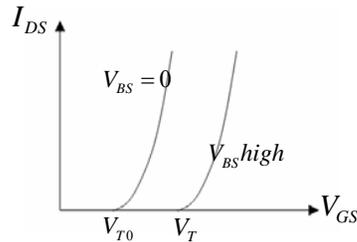
Fig 1.13

MOS transconductance as a function of overdrive and drain current

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## Deviation of I/V Characteristics



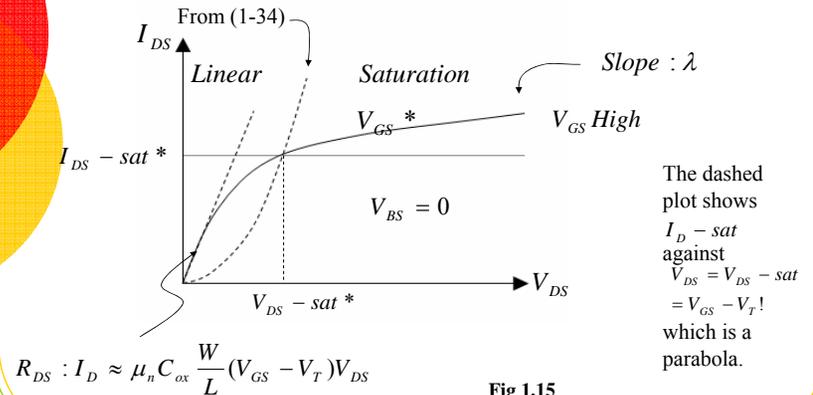
**Fig 1.14**  
Plot of  $I_{DS}$  versus  $V_{GS}$  &  $V_{BS}$

$$I_{DS} - sat = \frac{kp}{2n} \frac{W}{L} (V_{GS} - V_T)^2 \approx \frac{kp}{2n} \frac{W}{L} (V_{DS} - sat)^2 \quad (1-34)$$

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## Deviation of I/V Characteristics



**Fig 1.15**  
Plot of  $I_{DS}$  versus  $V_{GS}$  &  $V_{DS}$

$$R_{DS} : I_D \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS}$$

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## Channel Length Modulation

As  $V_{DS}$  increases beyond  $V_{DS} - sat$  as a result of the extension of the depletion layer charge at the drain into the channel toward the source (Fig 1.16) over a distance  $\Delta L$  the current is slightly increased. The voltage drop over  $\Delta L$  is about  $V_{DS} - sat$  so the channel length is reduced over a distance from  $L$  to  $L - \Delta L$ . This can be represented as follows:

$$I_{DS-sat} = \frac{kp}{2n} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda \cdot (V_{DS} - V_{DS-sat})) \quad (1-35)$$

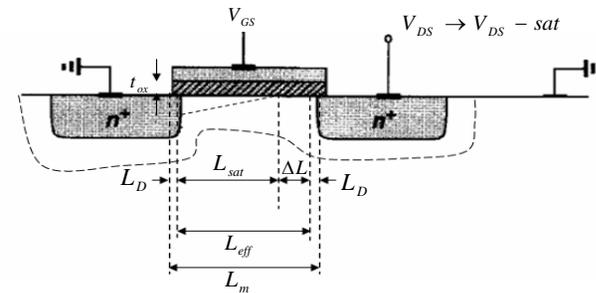
Unit: 1/V

Parameter  $\lambda$  depends on L (inversely).  
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## Channel Length Modulation



**Fig 1.16**  
Channel length modulation

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## Channel Length Modulation

### Effective channel length and width

The effective channel length  $L_{eff}$  given by

$$L_{eff} = L_m - 2L_D - \Delta L \quad (1-36)$$

Where  $L_m$  is the channel length drawn in the layout (on mask)  
 $L_D$  is the under diffusion and  
 $\Delta L$  is a reduction because of photolithography and etching

Similarly

$$W_{eff} = W_m + \Delta W \quad (1-37)$$

## Channel Length Modulation

Remember from (1-31):

$$\begin{aligned} g_m &= \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{V_{DS}=cte} \\ &= \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) = 2 \frac{k_p}{2n} \frac{W}{L} (V_{GS} - V_T) \\ &= \sqrt{2 \mu_n C_{ox} \frac{W}{L} I_D} = 2 \sqrt{\frac{k_p}{2n} \frac{W}{L} I_D} \\ &= \frac{2I_D}{V_{GS} - V_T} \end{aligned}$$

## Small signal parameters

### Bulk transconductance $g_{mb}$

From (1-30) and (1-19):

$$I_{DS} = \frac{k_p}{2n} \frac{W}{L} (V_{GS} - V_T)^2 = \frac{k_p}{2n} \frac{W}{L} (V_{GS} - [V_{T0} + \gamma(\sqrt{2|\Phi_F| - V_{BS}} - \sqrt{2|\Phi_F|})])^2$$

$$g_{mb} = \frac{\partial I_{DS}}{\partial V_{BS}} = \frac{\partial I_{DS}}{\partial V_T} \cdot \frac{\partial V_T}{\partial V_{BS}}$$

Recall

$$\gamma = \frac{\sqrt{2\varepsilon_{si}qN_{SUB}}}{C_{ox}}$$

$$n-1 = \frac{\gamma}{2\sqrt{\Phi_j - V_{BS}}} = \frac{1}{C_{ox}} \sqrt{\frac{\varepsilon_{si}qN_{sub}}{2(\Phi_j - V_{BS})}}$$

so  $\gamma$  is independent of  $V_{BS}$  and  
 $n$  is dependent on  $V_{BS}$

## Small signal parameters

$$\begin{aligned} \Rightarrow g_{mb} &= -2 \frac{k_p}{2n} \frac{W}{L} (V_{GS} - V_T) \cdot \frac{\partial V_T}{\partial V_{BS}} \\ &= -g_m \cdot \frac{\partial V_T}{\partial V_{BS}} = -g_m \left( -\gamma \cdot \frac{1}{2\sqrt{2|\Phi_F| - V_{BS}}} \right) \\ &= \frac{\gamma}{2\sqrt{2|\Phi_F| - V_{BS}}} \cdot g_m \quad (1-38) \end{aligned}$$

$$\text{From (1-11)} \quad g_{mb} = \frac{C_{BSQ}}{C_{ox}} g_m = (n-1)g_m \quad (1-39)$$

$$\Rightarrow n = 1 + \frac{g_{mb}}{g_m} \quad (1-40)$$

## Small signal parameters

**Note:**  $g_{mb}$  represents the transconductance from the bulk input-node voltage to the output current. It is actually the transconductance of the parasitic JFET.

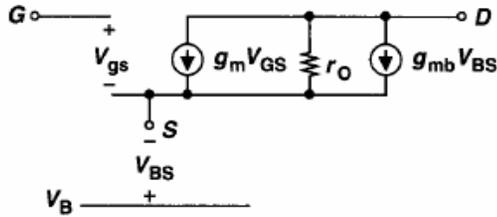


Fig 1.17  
Small signal model  
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## Small signal parameters

### Output Resistance $r_o$

It is the result of the channel-shortening effect by (channel length modulation).

$$g_o = \frac{\partial I_{DS}}{\partial V_{DS}} \approx \lambda I_{DSat} \quad (1-41)$$

$$\Rightarrow r_o = \frac{1}{\lambda I_{DSat}} \approx \lambda I_{DSat} \quad (1-42)$$

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## Small signal parameters

$$I_{DS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

Using Taylor approximation:

$$I_{DS} = I_{DS-sat} + \left[ \frac{\partial I_{DS}}{\partial L_{eff}} \cdot \frac{\partial L_{eff}}{\partial V_{DS}} \right] \Delta V_{DS}$$

$$\Rightarrow I_{DS} = I_{DS-sat} + \left\{ \frac{-\mu_n C_{ox} W}{2L_{eff}^2} (V_{GS} - V_T)^2 \right\} \cdot \left\{ \frac{\partial L_{eff}}{\partial V_{DS}} \right\} \cdot (V_{DS} - V_{eff})$$

$$L_{eff} = L - \Delta L = L - \sqrt{\frac{2k_{st} \epsilon_0}{qN_{SUB}}} \sqrt{\Phi_0 + V_{DS} - V_{eff}} = K_{DS} \sqrt{\Phi_0 + V_{DS} - V_{eff}}$$

$$\Rightarrow \frac{\partial L_{eff}}{\partial V_{DS}} = \frac{-K_{DS}}{2\sqrt{\Phi_0 + V_{DS} - V_{eff}}}$$

$$\Rightarrow I_{DS} = I_{DS-sat} \left( 1 + \frac{K_{DS}}{2L\sqrt{\Phi_0 + V_{DS} - V_{eff}}} \cdot V_{DS} - V_{eff} \right) \quad (1-43)$$

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## Small signal parameters

$$\Rightarrow I_{DS} = I_{DS-sat} (1 + \lambda (V_{DS} - V_{eff})) \quad (1-44)$$

where:

$$\lambda = \frac{K_{DS}}{2L\sqrt{\Phi_0 + V_{DS} - V_{eff}}}$$

$$r_o = \frac{1}{\lambda I_{DS}} = \frac{2L\sqrt{\Phi_0 + V_{DS} - V_{eff}}}{K_{DS} I_{DS}} = \frac{2L}{I_{DS}} \sqrt{\frac{qN_A}{2\epsilon_{si}}} (\Phi_0 + V_{DS} - V_{eff}) \quad (1-45)$$

**Note:**  $r_o \propto (L, \sqrt{V_{DS}})$

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## Small signal parameters

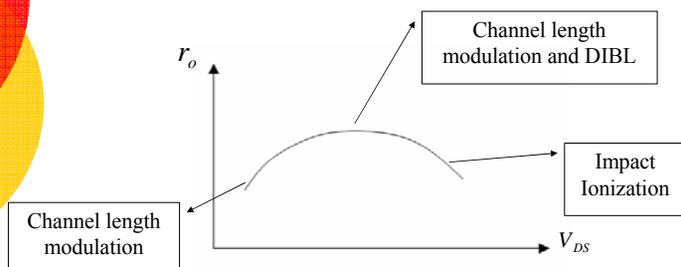


Fig 1.18

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## Small signal parameters

Parameter  $\lambda$  depends on the channel length  $L$ , yet assumed to be constant in spice. therefore another is chosen, taking into account the dependence on channel length  $L$ :

Equation (1-42) can be rewritten as follows:

$$r_o = \frac{1}{g_{ds}} = \frac{V_E \cdot L}{I_{Dsat}} \quad (1-46)$$

Comparing (1-42) and (1-46) :

$$V_E = \frac{1}{\lambda L} = \frac{V_A}{L} \quad (1-47)$$

$$\Rightarrow V_E = \frac{2\sqrt{(V_{DS} - V_{eff} + \Phi_0)}}{K_{DS}} \quad (1-48)$$

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## Small signal parameters

$V_E$  is the Early voltage per unit-channel length. in analogy with the Early voltage of a Bipolar transistor. It is different for nMOST and pMOST for the difference in substrate doping level:

**Note:** Early voltage is independent of  $L$

More doping level, the less extension of the depletion layer in to the channel  $\rightarrow$  the larger substrate doping, the larger the Early voltage.

Example:

N-well CMOS process:

For the same channel length, the output resistance of the nMOST is thus smaller than o the pMOST, in an n-well CMOS process.

It is opposite for a p-well CMOS process:

$$V_{Ep} = 4V/\mu mL; V_{En} = 7V/\mu mL$$

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## Small signal parameters

Another point of view:

$$I_D = \frac{k'}{2} \frac{W}{L} (V_{GS} - V_T)^2 \quad L_{eff} = L - X_d$$

$$\Rightarrow I_D = \frac{k'}{2} \frac{W}{L_{eff}} (V_{GS} - V_T)^2$$

$$\frac{\partial I_D}{\partial V_{DS}} = -\frac{k'}{2} \frac{W}{L_{eff}^2} (V_{GS} - V_T)^2 \cdot \frac{dL_{eff}}{dV_{DS}} = \frac{I_D}{L_{eff}} \cdot \frac{dX_d}{dV_{DS}} \quad (1-48)$$

So Early voltage is defined analogous to BJT

$$V_A = \frac{I_D}{\left(\frac{\partial I_D}{\partial V_{DS}}\right)} = L_{eff} \left(\frac{dX_d}{dV_{DS}}\right)^{-1} = \frac{1}{\lambda} \leftrightarrow \lambda = \frac{\left(\frac{dX_d}{dV_{DS}}\right)}{L_{eff}} \quad (1-49)$$

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## Small signal parameters

$$V_E = \frac{1}{\lambda L_{eff}} = \frac{1}{\left(\frac{dX_d}{dV_{DS}}\right)} \quad (1-50)$$

$$X_d = \sqrt{\frac{2k_s \epsilon_0}{qN_A}} \sqrt{(\Phi_0 + V_{DS} - V_{eff})} \quad (1-51)$$

$$\Rightarrow \frac{dX_d}{dV_{DS}} = \frac{K_{DS}}{2\sqrt{\Phi_0 + V_{DS} - V_{eff}}} \quad (1-52)$$

$$\Rightarrow \lambda = \frac{\left(\frac{dX_d}{dV_{DS}}\right)}{L} = \frac{K_{DS}}{2L\sqrt{\Phi_0 + V_{DS} - V_{eff}}} \quad (1-52)$$

$$V_E = \frac{1}{\lambda L} = \frac{2\sqrt{\Phi_0 + V_{DS} - V_{eff}}}{K_{DS}} \quad (1-53)$$

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## Small signal parameters

$$r_o^{-1} = \frac{\partial I_D}{\partial V_{DS}} = \frac{I_D}{L_{eff}} \frac{dX_d}{dV_{DS}} = \frac{I_D}{L_{eff}} \frac{K_{DS}}{2\sqrt{\Phi_0 + V_{DS} - V_{eff}}} \quad (1-54)$$

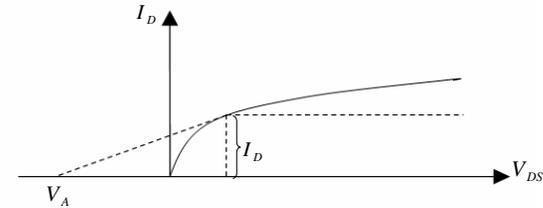


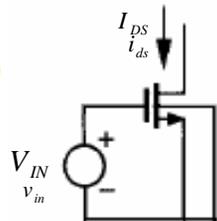
Fig 1.19  
Early Voltage

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## Small signal analysis examples

### Example 1



$$V_{T0} = 0.7\text{V}$$

$$\gamma = 0.86\text{V}^{1/2}$$

$$n = 1.49 (V_{BS} = 0)$$

$$k = \mu_n C_{ox} = 30 \mu\text{A}/\text{V}^2 = k_p/2n$$

$$\text{for } V_{IN} = 1.4\text{V}, \frac{W}{L} = \frac{50}{5}, v_{in} = 10\text{mV}_{rms}$$

$$\Rightarrow I_{DS}, i_{ds}, g_m, g_{mb}, r_o = ?$$

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## Small signal analysis examples

$$(1-30) \quad I_{out} = \frac{k_p}{2n} \frac{W}{L} (V_{GS} - V_T)^2 = 30 \times \frac{50}{5} (1.4 - 0.7)^2 = 0.147\text{mA}$$

$$(1-31) \quad g_m = 2 \left(\frac{k_p}{2n}\right) \frac{W}{L} (V_{GS} - V_T) = 2 \times 30 \times \frac{50}{5} (1.4 - 0.7) = 0.42\text{mS (Simens)}$$

$$(1-38) \quad g_{mb} = \frac{\gamma}{2\sqrt{2\Phi_F - V_{BSQ}}} g_m = \frac{0.86}{2\sqrt{2\Phi_F}} \times 0.42 = 0.206\text{mS}$$

$$\text{Note that } 2\Phi_F = 0.684\text{V}$$

$$\text{for } v_{in} = 10\text{mV}_{rms} \Rightarrow I_{out} = g_m v_{in} = 4.2\text{mA}_{rms} \rightarrow 4.2\sqrt{2} = 5.94\mu\text{A}$$

$$\text{for n-well process: } V_{En} = 4\text{V}/\mu\text{mL} \Rightarrow V_{En} \cdot L = (4\text{V}/\mu\text{mL}) \times 5\mu\text{m} = 20\text{V}$$

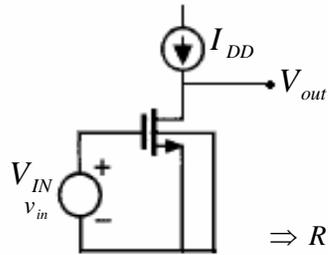
$$\Rightarrow r_o = \frac{V_{En} \cdot L}{I_{out}} = \frac{20}{0.147\text{mA}} = 136\text{k}\Omega$$

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## Small signal analysis examples

### Example 2: Amp with active load



$$\begin{aligned}
 V_{T0} &= 0.7\text{V} \\
 \gamma &= 0.86\text{V}^{1/2} \\
 n &= 1.49 (V_{BS} = 0) \\
 k &= 30 \mu\text{A}/\text{V}^2 \\
 \text{if } V_{DD} &= 8\text{V}
 \end{aligned}$$

$$\Rightarrow R_L = ? \quad \text{for } V_{out} = 8/2 = 4\text{V}$$

## Small signal analysis examples

$$R_L = \frac{V_{out}}{I_{DS}} = \frac{4}{0.15\text{mA}} = 27.2\text{k}\Omega$$

$$\Rightarrow R_L' = R_L \parallel r_o = 27.2 \parallel 136 = 22.7\text{k}\Omega$$

$$A_v = -g_m R_L' = -0.42\text{mS} \times 22.7\text{k}\Omega = -9.5\text{V}/\text{V}$$

from (1-33) and (1-46)

$$A_v = -g_m R_L = -\frac{2I_{DS}}{V_{GS} - V_T} \cdot \frac{V_{En} L}{I_{DS}} = -\frac{2V_{En} L}{V_{GS} - V_T} \quad (1-55)$$

The voltage gain is set by  $V_{GS}$  and  $L$  only (in strong inversion)

For high gain  $V_{GS} - V_T$  must be chosen smallest possible (0.2V) and  $L$  as large as possible.

$$L = 10 \mu\text{m} \Rightarrow |A_v| = \frac{2 \times 4\text{V}/\mu\text{m} L \times 10}{0.2} = 400\text{V}/\text{V} \rightarrow 52\text{dB}$$

## Small signal analysis examples

Determine  $W$ : The larger  $W$ , The larger  $I_{DS}$  and  $g_m$  but the smaller  $r_o$   
for  $W = 5 \mu\text{m}$

$$\Rightarrow \begin{cases} I_{DS} = 6 \mu\text{A}, g_m = 60\text{mS} \\ r_o = 6.7\text{M}\Omega \end{cases}$$

**Note:** Do not increase  $I_{DS}$  than necessary (for power consideration)

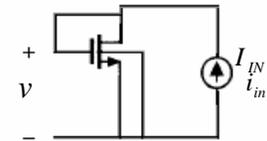
## Small signal analysis examples

### Example of MOST Diode

$$V_{GS} = V_{DS} \Rightarrow V_{DS} > V_{GS} - V_T$$

Always in saturation

There is no conduction for negative values so it is said to be a diode.

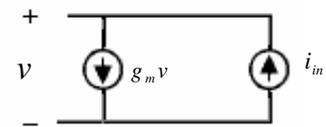


$$\text{for source grounded: } V_{GS} = V_T + \sqrt{\frac{I_{D-sat}}{k' W/L}}$$

Used for DC-shifter in MOS.

Voltage set by  $I$  and  $W/L$ .

AC voltage:  $i_{in}/g_m$

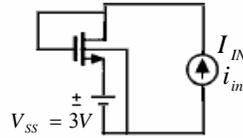


AC resistance is  $1/g_m$  (normally  $k_n$  shunted by  $k_p$ )  $\rightarrow$  still  $\approx 1/g_m$

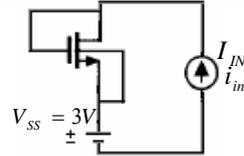
## Small signal analysis examples

### If using a voltage source:

if source is not grounded  $V_{bs}$  must be included for  $V_p$  calculation (1-10), so increasing  $V_{GS}$ . But  $g_m$  is not changed since is constant, (1-30), (1-31) and (1-32)!



For p-well process →



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## Small signal analysis examples

### Example (No Body Effect)

$$V_{T0} = 0.7V, \gamma = 0.86V^{1/2}, n = 1.49 (V_{BS} = 0)$$

$$k' = 30 \mu A/V^2, \frac{W}{L} = 50$$

$$\Rightarrow V_{DS} = V_{GS} = ? \text{ for } I_{in} = 0.2mA, AC_{swing} : 10\%$$

$$\Delta V = V_{DS} = V_{GS} = 0.7 + \sqrt{\frac{0.2mA}{30 \times 10^{-6} \times 10}} = 0.7 + \sqrt{0.667} \approx 1.52V$$

$$g_m = \frac{2I_{DSQ}}{V_{GS} - V_T} = 2\sqrt{k' \frac{W}{L} I_{DSQ}} = 2\sqrt{30 \times 10^{-6} \times 10 \times 0.2mA} = 0.49mS$$

$$\Rightarrow \frac{1}{g_m} = 2.04k\Omega$$

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## Small signal analysis examples

10% AC current:

$$I_{AC} = 0.10 \times (0.2mA) = 0.02mA$$

$$= g_m v_{in} \Rightarrow v_{in} = \frac{0.02mA}{0.49mS} = 40.8mV_p = 29mV_{rms}$$

### Example (With Body Effect)

$$\text{for } V_S = 3V \Rightarrow V_T = 0.7 + 0.86(\sqrt{0.6 + 3} - \sqrt{0.6}) = 1.66V$$

$$\Rightarrow \Delta V = V_{GS} = 1.66 + \sqrt{0.667} = 2.48V$$

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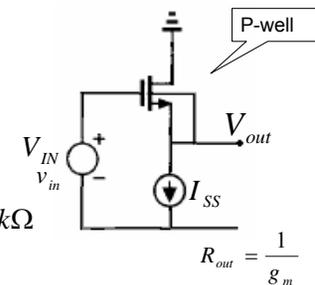
## Small signal analysis examples

### Examples of Source follower

$I_{SS}$  is constant so  $V_{GS}$  must be constant too:

$$V_{in} - V_{out} = V_{GS} \longrightarrow \boxed{AC + DC}$$

$$\text{Gate is @ AC ground} \Rightarrow R_{out} = \frac{1}{g_m} = 2.04k\Omega$$



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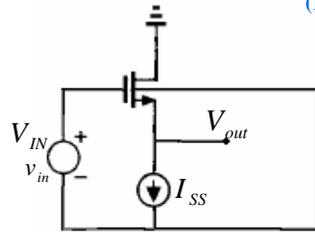
84

## Small signal parameters

For ground bulk:

$$V_{out} = V_{in} - V_{T0} - \gamma(\sqrt{2|\Phi_F| + V_{out}} - \sqrt{2|\Phi_F|}) - \sqrt{\frac{I_{SS}}{k'W/L}} \quad (1-56)$$

As it can be seen from (1-56) the gain is not unity! This is the result of the bulk effect or parasitic JFET.



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## Small signal parameters

We can draw the parasitic JFET explicitly (Drain and source are common with MOST but its gate i.e. bulk is grounded.).

$$\Rightarrow A_v = \frac{\frac{1}{g_{mb}}}{\frac{1}{g_m} + \frac{1}{g_{mb}}} = \frac{1}{1 + \frac{g_{mb}}{g_m}} = \frac{1}{n} \quad (1-57)$$

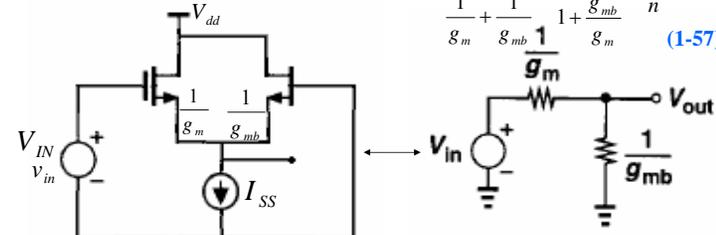


Fig 1.20a,b  
Parasitic JFET

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## Small signal parameters

**Description:** Consider the MOS T-Model (Fig 1.21)

Note that since  $i_s = g_m v_{gs}$  passes through  $r_s = \frac{1}{g_m}$ , so the current into gate (G terminal) is zero, thereby input impedance is infinity!

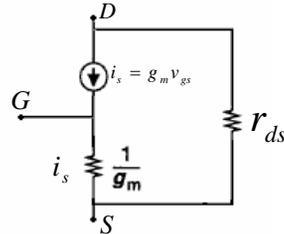


Fig 1.21  
MOS T-Model

So the AC small signal model of the circuit is really as shown in Fig 1.20b. Also the model is shown in Fig 1.22 (without  $r_{ds}$ )

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## Small signal parameters

**Note:** If  $V_{in} = 0 \Rightarrow V_{gs} = 0$  for  $V_{in} \neq 0$  we can calculate  $V_s$  as a voltage divider of  $1/g_m$  or  $1/g_{mb}$ . According to T-Model we know that in any case  $V_s$  is as follows (Fig 1.22):

$$i_s = g_m v_{gs}$$

$$\Rightarrow v_o = v_s = \frac{g_m v_{gs}}{g_{mb}} = \frac{g_m (v_{in} - v_o)}{g_{mb}} \quad (1-58)$$

$$\Rightarrow v_o \left(1 + \frac{g_m}{g_{mb}}\right) = \frac{g_m v_{in}}{g_{mb}}$$

$$\Rightarrow A_v = \frac{\frac{1}{g_{mb}}}{\frac{1}{g_m} + \frac{1}{g_{mb}}} = \frac{1}{1 + \frac{g_{mb}}{g_m}} = \frac{1}{n} \quad (1-59)$$

See(1-40)

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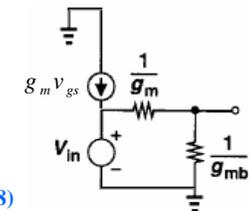


Fig 1.22

As shown  
before in  
(1.57)

## Small signal parameters

$$R_{out} = \frac{1}{g_m + g_{mb} + g_o} \approx \frac{1}{g_m + g_{mb}} \quad (1-60)$$

So bulk effect reduces gain and increases the  $V_{GS}$ !  
 It should be noted although we draw both voltage source, and current source, in T-Model in Fig 1.22 the current going through is always  $1/g_m$  equal to as shown in Fig 1.21.

## Example of MOST as a switch

### Resistive Load

$$\frac{V_{out}}{V_{in}} = \frac{R_L}{R_L + R_{DS}}$$

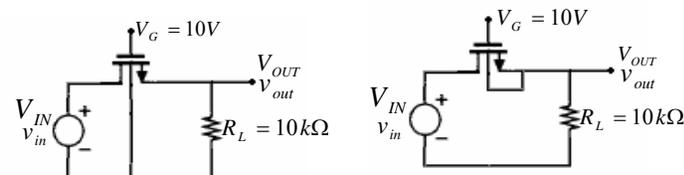


Fig 1.23a,b  
 MOST as switch with resistive load

## Example of MOST as a switch

We are in Triode region:

$$r_{ds} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T - V_{DS})} \quad (1-61)$$

From (1-10):

$$R_{DS} = \frac{1}{\beta [V_G - V_{out} - V_{T0} - \gamma(\sqrt{2}|\Phi_F| + V_{out} - \sqrt{2}|\Phi_F|)]} \quad (1-62)$$

where  $\beta = \mu_n C_{ox} \frac{W}{L}$

Since  $V_G$  is large  $R_{DS}$  is small, so  $V_{out} \approx V_{in}$

## Example of MOST as a switch

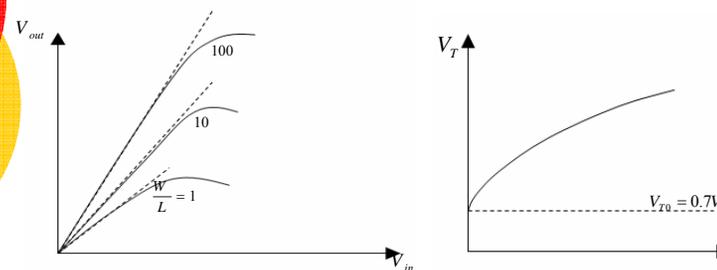


Fig 1.24a,b

## Example of MOST as a switch

- The larger the transistor, the smaller the resistance.
- The lower the input voltage, The smaller the resistance
- The value of threshold voltage increases with input voltage as shown in Fig 1.24b.(for  $V_{BS} \neq 0$  due to body effect)

## Example of MOST as a switch

### Capacitive Load

Used in switched capacitor and CMOS logics.

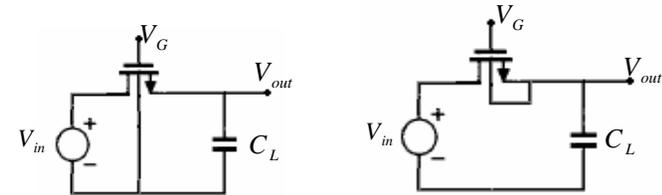


Fig 1.24a,b  
MOST as switch with capacitive load

## Example of MOST as a switch

$$V_{IN} = 1.4V, \frac{W}{L} = \frac{50}{5}, v_{in} = 10mV_{rms}$$

for

$$\Rightarrow I_{DS}, i_{ds}, g_m, g_{mb}, r_o = ?$$

(1-54)

Fig 1.19

## MOS Transistor as a switch

### Symbol



### On Characteristics of a MOS Switch

Assume operation active region ( $V_{DS} < V_{GS} - V_{TH}$  and  $V_{DS}$  is small). Thus:

$$R_{ON} = \frac{V_{DS}}{i_D} = \frac{1}{\mu C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{TH})}$$

### OFF Characteristics of a MOS Switch

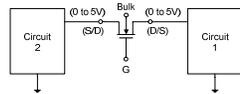
If  $V_{GS} < V_{TH}$ , then  $i_D = I_{OFF} = 0$  when  $V_{DS} \approx 0$ .

If  $V_{DS} > 0$ , then:

$$R_{ON} = \frac{1}{\lambda i_D} = \frac{1}{\lambda I_{OFF}} \approx \infty$$

## MOS Switch Voltage Range

If a MOS switch is used to connect two circuits that can have analog signal that vary from 0 to 5V, what must be the value of the bulk and gate voltages for the switch to work properly?



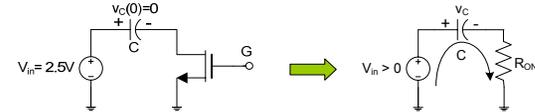
- > To insure that the bulk-source and bulk-drain pn junction are reverse biased, the bulk voltage must be less than the minimum analog signal for a NMOS switch.
- > To insure that switch is ON, the gate voltage must be greater than the analog signal pulse the threshold for a NMOS switch.

Therefore:  $V_{Bulk} \leq 0V$   
 and  $V_G > 5V + V_{TH}$   
 Also,  $V_G(OFF) \leq 0V$

Unfortunately, the large value of reverse bias bulk voltage causes the threshold voltage to increase.

## Influence of the ON Resistance on MOS Switches

Finite ON Resistance:



### Example:

Initially assume the capacitor is uncharged. If  $V_G(ON)$  is 5V and is high for 0.1μs, find the W/L of the MOSFET switch that will charge a capacitance of 10pF in five time constants

$$(K'_N = \mu_n C_{ox} = 110 \mu A/V^2 \text{ and } V_{TN} = 0.7 V)$$

## Influence of the ON Resistance on MOS Switches

### Solution:

The time constant must be equal to  $\frac{100ns}{5} = 20ns$  Therefore  $R_{ON}$  must be less than  $\frac{20ns}{10pF} = 2k\Omega$

The ON resistance of the MOSFET (for small  $V_{DS}$ ) is:

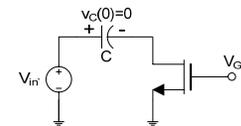
$$R_{ON} = \frac{1}{K'_N (W/L)(V_{GS} - V_{TH})} \Rightarrow \frac{W}{L} = \frac{1}{R_{ON} K'_N (V_{GS} - V_{TH})} = \frac{1}{2k\Omega \cdot 110 \mu A/V^2 \cdot 4.3} = 1.06$$

Comments:

- > It is relatively easy to charge on-chip capacitors with minimum size switches.
- > Switch resistance is really not constant during switching and the problem is more complex than above.

## Including The Influence of the Varying ON Resistance

### Gate-Source Constant:



$$g_{ON}(t) = K' \left( \frac{W}{L} \right) [(V_{GS}(t) - V_{TH}) - V_{DS}(t)]$$

$$g_{ON-av} = \frac{1}{\tau_{ON-av}} = \frac{g_{ON}(0) + g_{ON}(\infty)}{2}$$

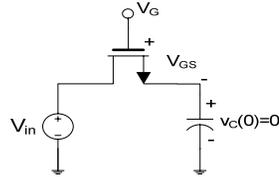
$$V_{DS}(\infty) = 0, V_{GS}(0) = V_{GS}(\infty) = V_{GS}$$

$$g_{ON-av} = \frac{K'}{2} \left( \frac{W}{L} \right) (V_{GS} - V_{TH}) - \frac{K'}{2} \left( \frac{W}{L} \right) V_{DS}(0) + \frac{K'}{2} \left( \frac{W}{L} \right) (V_{GS} - V_{TH})$$

$$= K' \left( \frac{W}{L} \right) (V_{GS} - V_{TH}) - \frac{K'}{2} \left( \frac{W}{L} \right) V_{DS}(0)$$

## Including The Influence of the Varying ON Resistance

### Gate-Source Constant:



$$g_{ON}(t) = K' \left( \frac{W}{L} \right) [(V_{GS}(t) - V_{TH}) - V_{DS}(t)]$$

$$g_{ON-avr} = \frac{1}{t_{ON-avr}} = \frac{g_{ON}(0) + g_{ON}(\infty)}{2}$$

$$g_{ON-avr} = \frac{K'}{2} \left( \frac{W}{L} \right) (V_{GS}(0) - V_{TH}) - \frac{K'}{2} \left( \frac{W}{L} \right) V_{DS}(0) + \frac{K'}{2} \left( \frac{W}{L} \right) (V_{GS}(\infty) - V_{IN} - V_{TH})$$

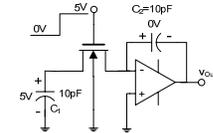
$$V_{DS}(\infty) = 0 = V_{GS}(\infty), V_{GS}(0) = V_{DD}$$

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## Switch ON Resistance Example

Assume that at  $t=0$ , the gate of the switch shown is taken to 5V. Design the  $W/L$  value of the switch to discharge the  $C_1$  capacitor to within 1% of its initial charge in 10ns. Use the MOSFET parameter for previous example.



### Solution:

Note that the source of the NMOS is on the right and is always at ground potential so there is no bulk effect as long as the voltage across  $C_1$  is positive. The voltage across  $C_1$  can be expressed as:

$$v_{C1} = 5 \exp\left(\frac{-t}{R_{ON} C_1}\right)$$

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## Switch ON Resistance Example

At 10ns,  $v_{C1}$  is 5/100 or 0.05V, therefore:

$$0.05 = 5 \exp\left(\frac{-10^{-8}}{R_{ON} 10^{-11}}\right) = 5 \exp\left(\frac{-10^3}{R_{ON}}\right) \Rightarrow \exp(G_{ON} 10^3) = 100$$

$$\Rightarrow G_{ON} = \frac{\ln(100)}{10^3} = 0.0046 \text{ S}$$

Note that the ON resistance is time variant:

$$G_{ON} = K' \frac{W}{L} [V_{DG}(t) - V_{TH}], \begin{cases} V_{DG}(0) = V_{DD} - 5V = 0 \\ V_{DG}(\infty) = V_{DD} - 0V = 5 \end{cases}$$

$$\therefore 0.0046 = K' \frac{W}{L} (V_{GS} - V_{TH}) - \frac{K'}{2} \frac{W}{L} V_{DS} = \left( 110 \times 10^{-6} \cdot 4.3 - \frac{110 \times 10^{-6} \cdot 5}{2} \right) \frac{W}{L}$$

$$= 198 \times 10^{-6} \frac{W}{L} \Rightarrow \frac{W}{L} = \frac{0.0046}{198 \times 10^{-6}} = 23.2 \approx 23$$

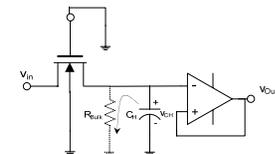
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## Influence of The OFF State ON Switches

The OFF state influence is primarily in any current that flows from the switch to ground.

An example might be:



Typically, no problems occur unless capacitance voltages are held for a long time. For example:

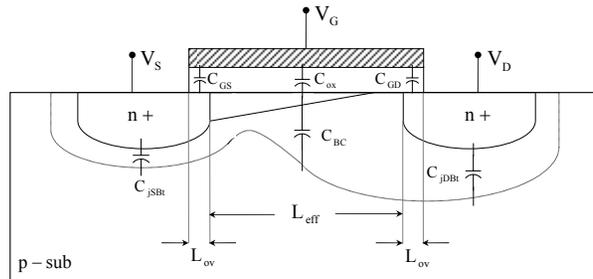
$$v_{out}(t) = v_{CH} [1 - e^{-t/(R_{Bulk} C_H)}]$$

If  $R_{Bulk} \approx 10^9 \Omega$  and  $C_H = 10 \text{ pF}$ , the time constant is  $10^9 \cdot 10^{-11} = 0.01 \text{ s}$ .

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## MOS Capacitances



## MOS Capacitances

$$C_{\text{ox}} = C_{\text{ox}} \cdot W \cdot L_{\text{eff}}$$

$$C_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}}$$

Oxide (isolation) Cap.

‡ stands for total

$$C_{\text{BCt}} = C_{\text{jBC}} \cdot W \cdot L_{\text{eff}}$$

$$C_{\text{jBC}} = \frac{C_j}{\left(1 - \frac{V_{\text{BC}}}{\phi_j}\right)^{m_j}}$$

Depletion Region Cap.  
(junction Cap.)

$$\phi_j = \phi_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

$\phi_j$  is the built-in potential of an open circuit pn junction. (PB)

## MOS Capacitances

$$C_{\text{jSBt}} = A_S \cdot C_{\text{jSB}} + P_S \cdot C_{\text{jswSB}}$$

$$C_{\text{jSB}} = \frac{C_j}{\left(1 - \frac{V_{\text{BS}}}{\phi_j}\right)^{m_j}}, \quad C_{\text{jswSB}} = \frac{C_{\text{jswSB}}}{\left(1 - \frac{V_{\text{BS}}}{\phi_{\text{jsw}}}\right)^{m_{\text{jsw}}}}$$

$$C_{\text{jDBt}} = A_D \cdot C_{\text{jDB}} + P_D \cdot C_{\text{jswDB}}$$

$$C_{\text{jDB}} = \frac{C_j}{\left(1 - \frac{V_{\text{BD}}}{\phi_j}\right)^{m_j}}, \quad C_{\text{jswDB}} = \frac{C_{\text{jswDB}}}{\left(1 - \frac{V_{\text{BD}}}{\phi_{\text{jsw}}}\right)^{m_{\text{jsw}}}}$$

$$C_{\text{jsw}} = \frac{\epsilon_{\text{si}}}{t_{\text{si}}} = \left(\frac{\epsilon_{\text{si}} q N_B}{2\phi_{\text{jsw}}}\right)^{1/2}, \quad t_{\text{si}} = \text{Thickness of Depletion Layer}$$

$$m_j = m_{\text{jsw}} = 1/3, \dots, 1/2$$

$A_S$  is the Source area, and  $P_S$  is the Source perimeter.

$A_D$  is the Drain area, and  $P_D$  is the Drain perimeter.

## MOS Capacitances

### In Saturation Region

$$C_{\text{GS}} = C_{\text{GSov}} + 2/3 C_{\text{ox}}$$

$$C_{\text{GD}} = C_{\text{GDov}}$$

$$C_{\text{SB}} = C_{\text{jSBt}} + 2/3 C_{\text{BCt}}$$

$$C_{\text{DB}} = C_{\text{jDBt}}$$

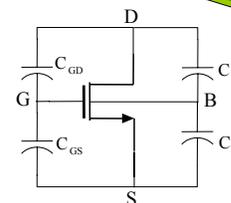
Overlap Capacitance between Gate and Source

Overlap Capacitance between Gate and Drain

Channel-Bulk junction Capacitance

Source-Bulk junction Capacitance

Drain-Bulk junction Capacitance



## MOS Capacitances

- **In Triode (linear) Region**

$$C_{GS} = C_{GDov} + 1/2 C_{oxl}$$
$$C_{GD} = C_{GDov} + 1/2 C_{oxl}$$
$$C_{SB} = C_{jSBt} + 1/2 C_{Bct}$$
$$C_{DB} = C_{jDBt} + 1/2 C_{Bct}$$

