27.8 A Continuous Time ΔΣ ADC for Voice Coding with 92dB DR in 45nm CMOS

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In modern technologies, the impressive digital device performance is accomplished at the cost of analog design features. The prediction of the ITRS roadmap [1] shows a dramatic increase of flicker noise in new technologies. On the other hand, the voltage supply is reduced to almost 1V. This paper wants to clarify the important design parameters of the 45nm process like matching, flicker noise, and offset from an analog designers' point of view.

In comparison to any other basic analog building blocks, a multibit CT ΔΣ ADC is uniquely well suited for separating all relevant device imperfections. Its current-steering DAC provides spectral information (harmonics) about dynamic MOS transistor mismatch. The SC quantizer reveals dynamic mismatch of capacitances. In addition to that, the optional chopped filter input stage open the possibility to separate flicker noise of weakly and strongly inverted transistors. Beyond the analog performance, excess loop delay and jitter, which represent the digital performance of the circuitry, can be seen in the power spectral density (PSD) plot.

Figure 27.8.1 shows the feedback topology of the CT ΔΣ ADC [2, 3]. It consist of a 2nd-order loop filter, a tracking quantizer, and 2 current-steering feedback DACs as described in [3]. The OSR is 300, the clock frequency is 12MHz and the filter coefficients are the same as in the 65nm design. The feedback DACs are optionally linearized by means of dynamic element matching [6]. The first stage of the first opamp has to be chopped to reduce flicker noise and offset [5]. In this 45nm design, the bandwidths of the opamps are reduced in comparison to the 65nm design [3] in order to lower the power consumption.

The DAC-cell topology of the first and second feedback DAC and the bias circuit are shown in Fig. 27.8.2. Low-noise and matching requirements lead to a long shaped current transistor (MPC, MNC) with a high overdrive voltage. Due to the large area of the devices, gate leakage current of the 45nm transistors are not negligible anymore causing different mirror ratios of NMOS and PMOS mirrors. Thanks to the differential structure of the architecture, the ADC is insensitive to this effect. Otherwise, bipolar design techniques had to be used. Operating from a 1.1V supply, there is no voltage headroom for cascode transistors anymore. With the pessimistic preliminary transistor noise parameters, the bias and the DAC contribute a huge amount of the core area, and also to the current consumption. All switches in the core are of minimum length. They benefit from the technology shift.

Based on [7], the tracking ADC [4] is modified for low-voltage applications (Fig. 27.8.3). In the previous design, there was an R string reference ladder with 15 transmission gates to the input of the comparator. These transmission gates are switching voltages near the middle of the supply range and create long time delays that limits the speed of the quantizer. At low supply voltage, imposed by the 45nm technology, this technique is not feasible anymore. Therefore, the R string DAC is replaced by capacitive voltage divider. At the beginning of the conversion phase, all switches are connected either to the positive reference, V_{refp} (near V_{DD}), or the negative reference, V_{refn} (near ground), which creates a code-independent short settling.

The measured output spectrum density plots are shown in Fig. 27.8.4. The top diagram depicts the spectra for large signals. The input sine frequency is 1,052kHz and the input amplitude is -3.8dBFs (0dB Full Scale=1.32$V_{pp\text{-}diff}$). The chopping has almost no impact on the SNR or the SNDR. Chopping creates no idle tones within the band of interest. The measurements are done with and without chopping of the first stage of the filter. The chopper frequency is at 46kHz and is programmable from 23 to 375kHz. The bottom graph shows the idle channel noise (ICN) measurements. The integrated in-band noise is -91.7dBFs (-88.5 without chopping). The remaining flicker noise is caused by the DAC. The flicker noise is smaller than what was expected from simulation. The pessimistic preliminary transistor parameters results in large core area, a chopped first integrator, and a large supply current. Compared with the previous design, this test chip demonstrates almost no degradation in flicker noise although the area is reduced by 30% and the current is cut in half. Consequently, the preliminary noise parameters are overly pessimistic and can be relaxed to avoid power and area waste. Despite the low intrinsic gain of transistors in 45nm, it is sufficient to use a 2-stage opamp with cascoded input stages to achieve a DR in the order of >90dB. In this 45nm design, the chopping spur of -45dB is much larger than -90dB in the reference design described in [3]. Even though just a few samples are measured, this is an indication of a dramatic increase of the mismatch and offset voltage. The SNR, SNDR and SNDR without DWA, are depicted in Fig. 27.8.5 as a function of the input-signal amplitude. The peak SNR of 78.7dB (77.9 without chopping) is achieved with a maximum input signal of 3.8dBFs. In .Fig. 27.8.4, the SNDR without dynamic element matching is given to verify the shuffling circuitry. The noise increases in the presences of a signal, lowering the DR to -85dBFs.

The chip is fabricated in a standard digital 45nm CMOS technology. No additional devices, like low-V_T transistors are used in this design. The design is compared with the previous implementation in 65nm technology in Fig. 27.8.6. The unoccupied area is filled with blocking capacitors. The area occupied due to noise requirements in the fist integrator stage (38%), in the biasing (28%) and in the first DAC (13%) is almost 4/5 (79%) of the core. A performance summary and a comparison are shown in Fig. 27.8.7. As a result, analog design with small areas and large DR is possible without using chopping techniques. Offset and matching is getting worse, but flicker noise is almost the same as indicated in the 65nm reference design. As a consequence, 45nm designs can be profitably applied to analog mixed-signal products, even though some circuit blocks have to be adapted to low supply voltages in an innovative way.

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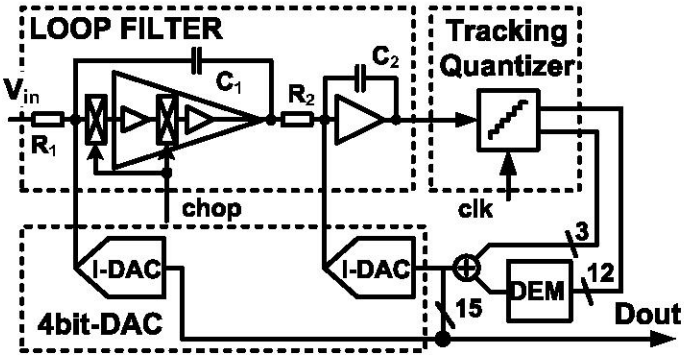

Figure 27.8.1: 2nd-order 4b CT ΔΣ ADC architecture.

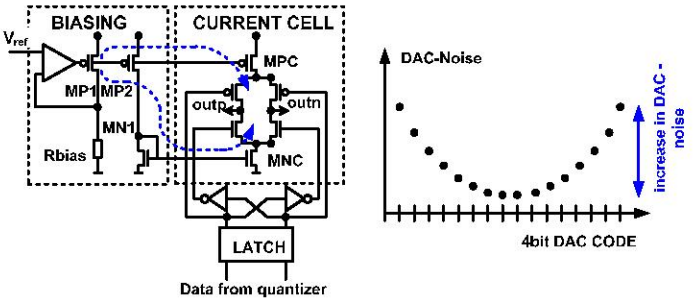

Figure 27.8.2: Implementation of one DAC cell and biasing.

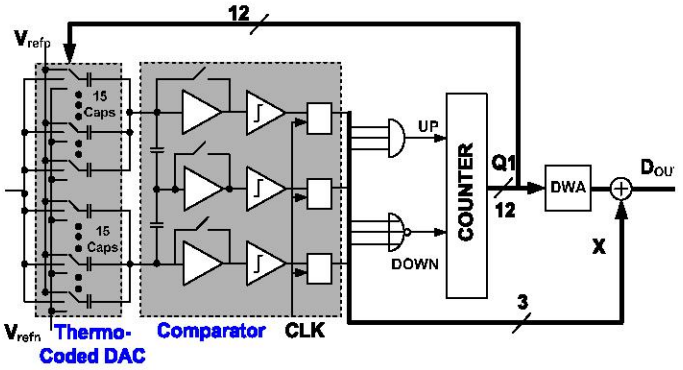

Figure 27.8.3: Tracking ADC with capacitive voltage reference DAC.

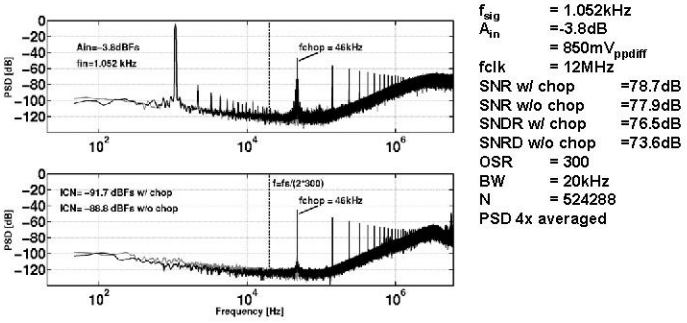

Figure 27.8.4: Measured output spectrum with / without chopping.

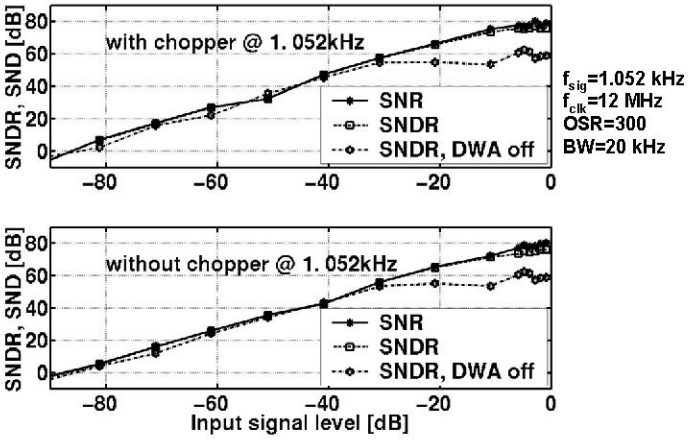

Figure 27.8.5: SNR versus input signal.

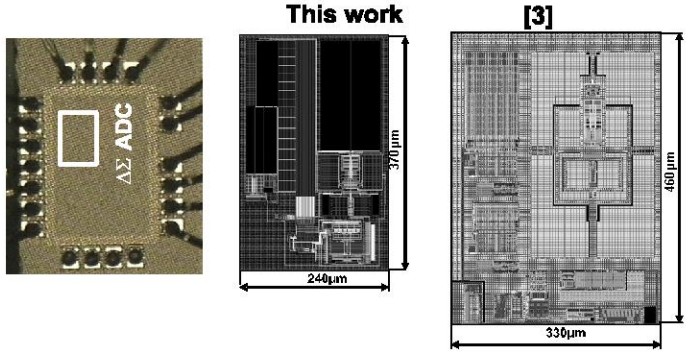

Figure 27.8.6: ADC-core layout & chip micrograph comparison.

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	This work	[3]
Power Supply Voltage	1.1V	1.2V
Signal Bandwidth	20 kHz	20 kHz
Sampling Frequency	12 MHz	12 MHz
Oversampling Ratio	300	300
Power consumption	1.2mW	2.2mW
Max. diff. input Level	1.32 V_{ppdiff} (0dB Fs)	1.4V_{ppdiff} (0dB Fs)
Peak SNR w/ w/o chopping	78.7dB / 77.9dB [1]	77.0dB [2]
Peak SNDR w/ w/o chopping	76.5dB / 73.6dB [1]	74.0dB [2]
Peak THD w/ w/o chopping	80.5dB / 77.5dB @ -3.8dBFs [1]	82.0dB @ -30dBFs [2]
Dynamic Range w/ w/o chopping	91.7dB / 88.8dB [1]	95.0dB [2]
Core Area	0.0895 mm^2	0.149 mm^2
Technology	45nm low power	65nm low power

[1] Measured at 1.052 kHz

[2] Measured at 4.85 kHz, unchopped mesurements not available

Figure 27.8.7: Performance Summary.

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