A New Digital Multiple Feedback Control Strategy for Single-phase Voltage-source PWM Inverters

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***Abstract*--This paper proposed a new digital multiple feedback control for uninterruptible power supply (UPS) with single-phase half-bridge inverter. The control scheme is based on sensing the current and voltage of the of the filter's capacitor. Thus current deadbeat control is achieved, which is easy to be deduced by discrete state equation of the LC filter. Then an outer voltage feedback loop with fuzzy control is also used to ensure load voltage to be sinusoidal and well regulated. It is shown the control scheme which is simple and can be designed easily offers improved performance over the traditional deadbeat control especially with nonlinear load. Simulation and experimental results based on TMS320F240 (DSP) proved it.**

***Index Terms*—deadbeat control, fuzzy control, multiple feedback, UPS**

I. INTRODUCTION

UPS are used to interface critical loads such as computers and communication system to the utility system. The output voltage of the UPS inverters is required to be sinusoidal with minimum total harmonic distortion. SPWM scheme, which is used to depress low order harmonics, is the most important way to achieve "clean" sinusoidal waveform. However, this scheme including optimum PWM scheme to eliminate harmonics can't suppress the distortion under nonlinear loads.

To over this drawback, many control strategies are proposed such as PID control, instantaneous feedback control, sliding mode control, repetitive control and so on [1][2]. It is difficult to have both excellent transient response and low THD of output waveform because the waveform is influenced by many facts:

(1). The load is changeable especially nonlinear load that causes intense current disturbance.

(2). SPWM modulation is not an ideal amplification including dead-time and conducting resistance of device.

With the development of microprocessor and digital signal processor (DSP), the control scheme is demanded to be numeric because of its high reliability, coincidence and flexibility. But it is difficult to transform analog control into digital control because of the limit of sampling frequency and time lag of calculation.

Deadbeat control is applied into power electronics in the middle 1980's [3]. It is a digital control method with fast response and precise tracking reference with linear load by real time calculating the pulse width of the next switch period at each sample time. Then deadbeat control with load disturbance observer is proposed which in some distance solved the waveform distortion with capacitor feed rectifier [4]. But this scheme demanded relatively large filter capacitor to compensate the error between predicted load current and real load current.

A new control scheme has been proposed in [5]. In this technique the current in the filter capacitor is used as the feedback variable to achieve sinusoidal capacitor current. An outer voltage current loop is also used for load voltage regulation and compensation for perfection in the implementation of current control loop.

But it is a kind of analog control. In order to achieve digital multiple feedback, a robust digital control was proposed [6]. Though there are excellent experimental result shown in this paper, it is a little complex to achieve the algorithm because the current sampling frequency is as high as two times the PWM carrier frequency and two observers is to be accomplished.

This paper proposed a new algorithm of digital multiple feedback control that is simple and can be designed easily. The inner loop is achieved by deadbeat control that is easy to be deduced by discrete state equation. The outer loop can adopt a proportional compensator because of the fast response of the inner loop. In order to increase the voltage loop adaptive ability and the stability, fuzzy control is adopted to achieve various proportional compensator according to the error between the reference and output voltage.

Theoretical analysis and experiments show the validity of the proposed method. The scheme is implemented by TMS320F240 (DSP) and the sampling frequency is 20kHz.

II. THE PROPOSED CONTROL SYSTEM

Fig.1 shows the circuit of the single-phase half-bridge voltage source UPS inverter. It mainly consists of inverter-bridge,

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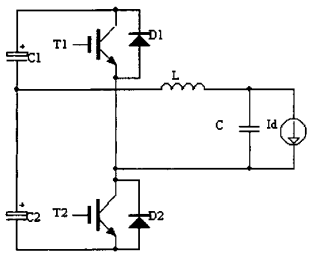


Fig.1 Circuit of the single-phase half-bridge inverter

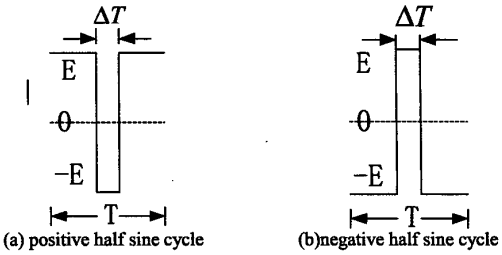


Fig.2 Two-level PWM pattern

output filter and load. If the load current I_d is regarded as step disturbance and the deadtime is neglected with the equivalent resistive of the inductor and capacitor, the ideal system state equation is:

$$\begin{bmatrix}\dot{V}_C\\ \dot{I}_C\end{bmatrix}=\begin{bmatrix}0 & \frac{1}{C}\\ -\frac{1}{L} & 0\end{bmatrix}\begin{bmatrix}V_C\\ I_C\end{bmatrix}+\begin{bmatrix}0\\ \frac{1}{L}\end{bmatrix}V_i \qquad (1)$$

$$y=[1,0]x$$

V_i is the inverter bridge output. To a half bridge inverter (Fig.1), V_{in} has only two values: +E or –E. The discrete-time system equation of two-lever switching pattern shown in fig.2 is deduced in [7].

Thus the discrete state equation is:

$$\mathbf{X}(k+1)=\Phi X(k)-\mathbf{G}*\Delta T+\mathbf{H} \qquad (2.a)$$

$$\mathbf{X}(k+1)=\Phi X(k)+\mathbf{G}*\Delta T-\mathbf{H} \qquad (2.b)$$

Where:

$$\begin{cases}\Phi=e^{\mathbf{A}T}=\begin{bmatrix}\Phi_{11} & \Phi_{12}\\ \Phi_{21} & \Phi_{22}\end{bmatrix}\\ \mathbf{G}=2e^{\mathbf{A}T/2}\begin{bmatrix}0\\ 1/L\end{bmatrix}E=\begin{bmatrix}g_1\\ g_2\end{bmatrix}\\ \mathbf{H}=\mathbf{A}^{-1}(e^{\mathbf{A}T}-\mathbf{I})\begin{bmatrix}0\\ 1/L\end{bmatrix}E=\begin{bmatrix}h_1\\ h_2\end{bmatrix}\end{cases}$$

Equation (2.a) and (2.b) is corresponding to the two-lever PWM pattern shown in fig.2 respectively. For convenient, this paper will analysis the control system with (2.a), which actually is no difference with (2.b).

Take first row of (2.a) and let $V_C(k+1)=V_C^*(k+1)$, then

$$\Delta T=\frac{V_C^*(k+1)-\Phi_{11}V_C(k)-\Phi_{12}I_C(k)-h_1}{g_1} \qquad (3)$$

This is the traditional state feedback deadbeat control. The pulse width is determined by (3) at every sample time, so the system has very fast response for load disturbance. But if the load is rectifier with capacitor, the THD would increase greatly.

According to (2.a), if take the second row and the current deadbeat control is achieved as follow:

$$\Delta T=\frac{I_C^*(k+1)-\Phi_{21}V_C(k)-\Phi_{22}I_C(k)-h_2}{g_2} \qquad (4)$$

Equation (4) has the same meaning as (3), that is $I_C(k)$ lags $I_C^*(k+1)$ by one sampling time, so that the filter's capacitor current track the reference sinusoidal current, which means that the inner loop has fast response. Fig.3 shows the inner loop block diagram.

But what we need is the sinusoidal output voltage, the outer voltage loop is inevitable. 1) It is difficult to attain precise value of the parameter L and C. 2) I_d is regarded as step disturbance, which causes unacceptable error if the load is rectifier with large capacitor leading intense current change. That is to say, the outer loop should have the ability to suppress the model error. Generally speaking, simple proportion adjustor can be adopted to compensate the voltage error. But if it is nonlinear load, constant proportion adjustor is difficult to promise low THD. If the proportion were increased, the system stability would be influenced. Therefor, fuzzy logical control (FLC) is introduced in this paper.

FLC is a kind of automatic control system that based on fuzzy mathematics, knowledge expression in fuzzy linguistic

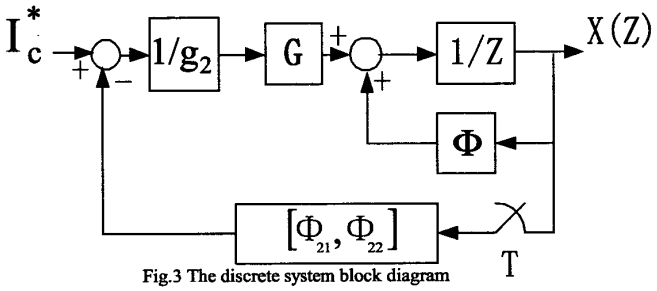


Fig.3 The discrete system block diagram

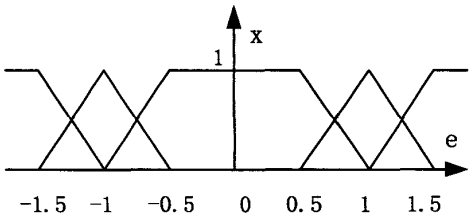


Fig.4 Member ship function for fuzzy and defuzzy

statement and knowledge inference in fuzzy logic. It is a kind of digital control system with closed-loop feedback, and its essence is fuzzy controller.

FLC has the following advantages:

(1) It can work with less precise input.

(2) The algorithm is simple and it doesn't need advanced processor.

(3) It needs less data storage in the form of membership function and rules than conventional look up table.

(4) It is robust.

Fig.4 shows the membership function used in this scheme. Error between reference and output can be labeled as negative zero (NZ), negative small (NS), negative big (NB), positive zero (PZ), positive small (PS), positive big (PB). A typical rule can be written as:

R: If E is A_i, then C_i.

And the center of gravity method is used to calculate the fuzzy output.

$$K=\frac{\sum C_i X_i}{\sum X_i} \qquad (5)$$

Where: A_i is the fuzzy rules table.

X_i is the degree of membership function.

K is the outer loop proportional gain.

III. System Stability and Transient Response

It is well known that the condition of discrete system stability is that all the poles must be in unit circle. In order to simply the system, the inner loop is first analyzed.

The inner loop transfer function is:

$$\frac{X(Z)}{I_C^*(Z)}=[ZI-\Phi+G[f_{21}\quad f_{22}]/g_2]^{-1}\begin{bmatrix}\frac{g_1}{g_2}\\1\end{bmatrix} \qquad (6)$$

$$=\begin{bmatrix}Z-\Phi_{11}+\frac{g_1}{g_2}\Phi_{21} & -\Phi_{12}+\frac{g_1}{g_2}\Phi_{22}\\0 & Z\end{bmatrix}^{-1}\begin{bmatrix}\frac{g_1}{g_2}\\1\end{bmatrix}$$

Then:

$$\frac{I_C(Z)}{I_C^*(Z)}=\frac{X_2(Z)}{I_c^*(Z)}=\frac{Z-\Phi_{11}+g_1\Phi_{21}/g_2}{Z(Z-\Phi_{11}+g_1\Phi_{21}/g_2)}=\frac{1}{Z} \qquad (7)$$

From (7), the inner state feedback law achieves pole-zero cancellation and the other pole is at the origin of Z-plane. So the actual capacitor current is lagging reference with one sampling time.

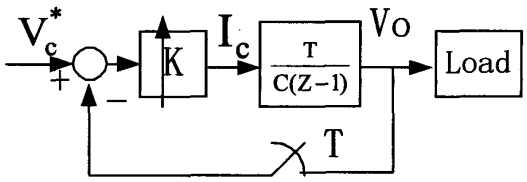


Fig.5 The equivalent outer loop

Therefore, the inner loop can be simplified the equivalent system block diagram is shown in fig.5. Then the transfer function is:

$$G(Z)=\frac{\frac{KT}{C(Z-1)}}{1+\frac{KT}{C(Z-1)}}=\frac{KT/C}{Z-1+KT/C} \qquad (8)$$

Obviously, $|Z|<1$ is the condition for stability. If $K=\frac{C}{T}$, then $G(Z)=\frac{1}{Z}$. That is to say, the voltage deadbeat control will be achieved. But actually, the precise system model is difficult to attain and the delay of disturbance detection is inevitable. On the other hand, the value of K will influence the system stability and output precision. Now, K is changed according to the former fuzzy rules. If the absolute of error is small, K is small; if the absolute of error is large, K is increased. Table.1 shows the rule table that is a little difference with other fuzzy rule table.

error	NB	NS	NZ	PZ	PS	PB
K	PB	PS	PZ	PZ	PS	PB

Table.1 Rule table

IV. Simulation and Experimental Result

Computer simulation of the half-bridge inverter system controlled by the modified deadbeat control algorithm is carried out to study the output characteristics. The parameter of the circuit is:

Sampling interval=T=50uS

Reference sinusoidal wave =50Hz, 100V (peak)

DC bus voltage=300V

Rated load resistance=5 Ω

Fig.6, fig.7 and fig.8 show the simulation output waveform of voltage and current under resistive load, sudden step load and capacitor with large capacitor respectively. The THD of the voltage in fig.6 and fig.8 is 0.2% and 1.26% respectively.

TMS320F240 has the architecture features necessary for high-speed signal processing and digital control functions, and it has the peripherals to provide a single-chip solution for motor control and inverters. Here, it is used to achieve the proposed control scheme.

Fig.9 shows the output voltage waveform with no load and its THD=1.11%. Fig.10 shows the output voltage and current waveform with rectifier load and voltage THD=2.7%.

The resean that the THD of experiment result is higher than the simulation is:

(1). SPWM modulation is not an ideal amplification including dead-time and conducting resistance of device. But the simulation is achieved under ideal mathematical model.

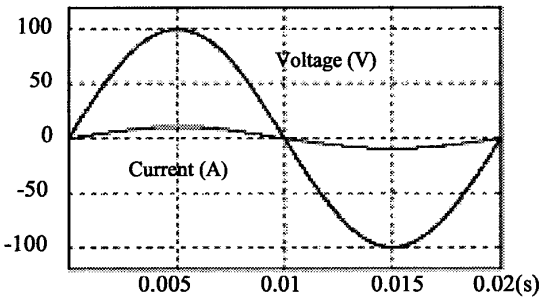


Fig.6 Simulation waveform of the output voltage and current with resistive load (R=10 Ω)

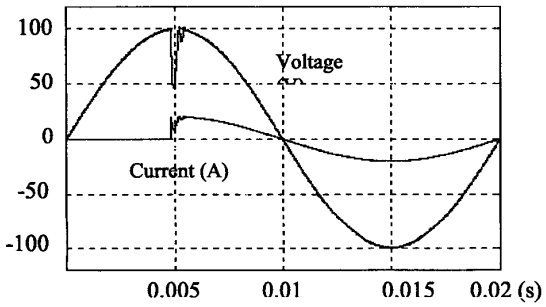


Fig.7 Simulation waveform of the output voltage and current with sudden step load (R= ∞ → 5Ω)

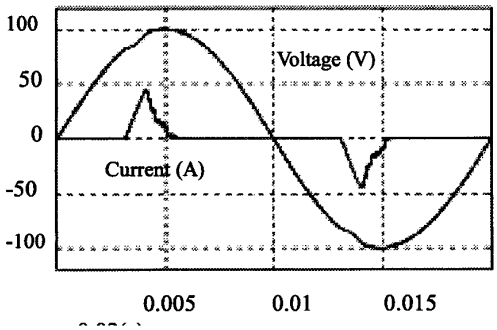
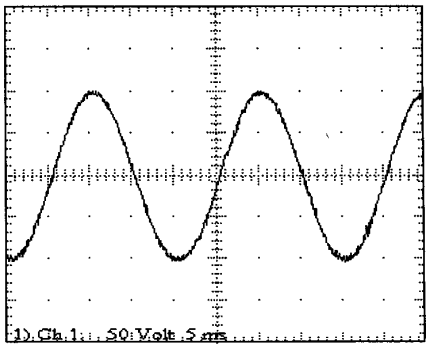


Fig.8 The output voltage and current waveform feeding with capacitor-resistive rectifier



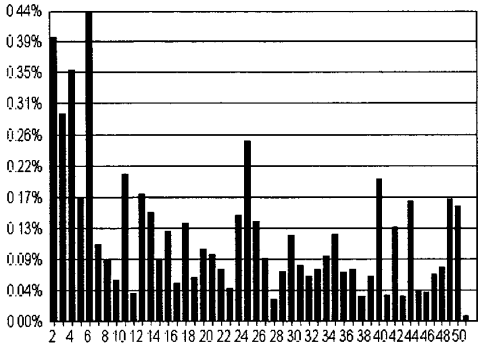


Fig.9 Output voltage waveform and harmonic magnitude of the fundamental amplitude

(2). The precision of TMS320F240's A/D converter is a little lower because it has only 10 bits which means that the outer voltage error proportion can't be too large.

(3). The state observer can also generate error.

V. Conclusion

A fast response digital control method for the inverter was presented. The performance of state observer and high sampling frequency obtained by asymmetric regular sample allowed the proposed method to achieve quick and exact current control. The method is fit for full digitalization of small capacity UPS.

References

[1] Kang Yong, "Study of Control Techniques of Output Voltage of High Frequency & High Power SPWM Inverter," *Doctor's Degree Dissertation of Huazhong University of Sci. & Tech. (in Chinese),* 1994

[2] T.Haneyoshi, A.Kawamura, and R. G. Hoft, "Waveform compensation of PWM inverter with cyclic fluctuating loads," *IEEE Trans. Ind. Applicat.*, vol.24, pp582-589,1988

[3] K. P. Gokhale, A. Kawamura and R. G. Hoft, "Deadbeat Microprocessor Control of PWM Inverter for sinusoidal Output Waveform Synthesis," *pp.28-36, IEEE-PESC'85* , 1985

[4] T. Yokoama and A. Kawamura, "Disturbance Observer Based Fully Digital Controlled PWM Inverter for CVCF Operation," *pp473-480. IEEE Trans. Power Electron.*, No.5, 1994

[5] N. R. Zargari, P. D. Ziogas and G. Joos, "A two switch high performance current regulated DC/AC converter module," *Proc. IEEE Industry Applications Society Ann. Meet. 1990,* pp.929-934

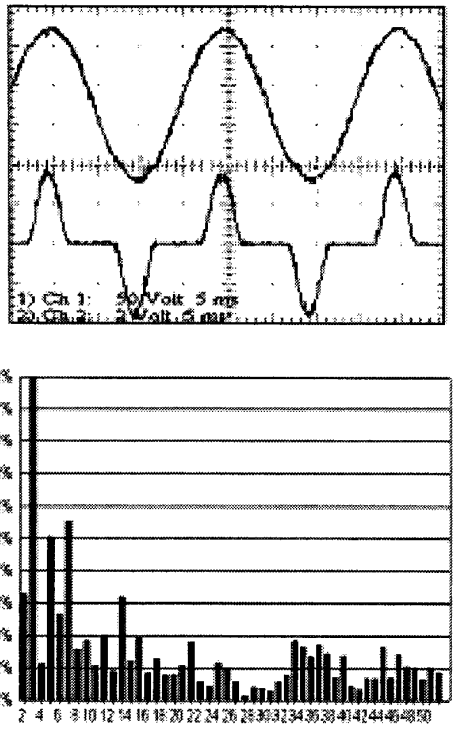


Fig.10 Output voltage and current waveform with rectifier load and voltage harmonic magnitude of the fundamental amplitude (current: 10A/div)

[6] Y. Ito and S. Kawauchi, "Microprocessor-Based Robust Digital Control for UPS with Three-Phase PWM Inverter" pp196-293, *IEEE Trans. Power Electron.*, No.2, 1995, *IEEE-PESC'85*

[7] Chihchiang Hua, "Two-Lever Switching Pattern Deadbeat DSP Controlled PWM Inverter" *IEEE Trans. Power Electron.* Vol.10. No.3. pp.310-317, May 1995.

[8] Yasuhiko Miguchi, Atsuo Kawamura and Richard G. Hoft, "Optimal pole assignment for power electronic Systems" *pp.74-88, IEEE-PESC'85*

[9] B. K. Bose, "Expert system, fuzzy logic,and neural network applications in power electronics and motion control," *Proc. IEEE*, vol.82, no.8, pp.1303-1325,1994.

[10] Texas Instruments, "TMS320C24x DSP Controllers: peripheral library and specific devices."