A Dual-Band CMOS CDMA Transmitter Without SAW and Driver Amplifier

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***Abstract*—A SAW-less dual-band I/Q transmitter without a Driver Amplifier (DA) is designed for dual-band (PCS/IMT, cellular) CDMA applications. The receive band noise is better than -159 dBc/Hz. It can provide up to +5 dBm output power and meets the ACPR and dynamic range requirements of both PCS/IMT and cellular CDMA. The measured S_{22} is better than -10 dB for both bands and it requires no external matching components. The transmitter is implemented in a 65nm digital CMOS technology, and is packaged using flip-chip technology. The transmitter signal path (RF portion) occupies 1.0 mm^2.**

***Index Terms*—Driver Amplifier (DA), up-converter, SAW filter, SAW-less transmitter, SSB mixer, Gilbert cell mixer, switched-transconductance mixer, gain control, CDMA, ACPR, LO-leakage.**

I. Introduction

An important challenge toward integration of any transceiver is removing the off-chip SAW filter between the up-converter and the PA, which is used to reduce the transmitter noise that overlaps with the receive band [1], [2]. A typical CDMA transceiver is shown in Fig. 1. As shown in this figure, the duplexer provides 50 dB attenuation of the transmitter noise at the receive band. In a SAW-less approach, the transmitter noise must be lower than -155 dBc/Hz in the receive band to prevent degradation of the receiver Noise Figure (NF) due to the transmitter noise [3].

The off-chip Power Amplifiers (PA's) do not contribute significantly to this noise [4] while the on-chip Driver Amplifiers (DA's) are a major contributer. So, the key to eliminating the SAW filter in a CDMA transmitter is reducing the noise of the on-chip circuits. The transmitter in [5] uses an LO generation scheme along with auto-calibration to reduce the noise of the mixer. In the transmitter of [4], a feedback cancellation method is employed to suppress the noise of the on-chip DA. A pulsing technique is used in [3] to achieve switching patterns to reduce the noise of the mixer.

Eliminating the DA brings several benefits: (1) it reduces the transmitter noise in the receive band and this enables SAW-less operation. (2) A DA-less design leads to removing all the external matching components since in the DA-less design the up-converter balun is used for matching. So it will save PCB area. (3) Removing the DA reduces the die area.

Removing the SAW filter usually requires an increase in the dc current of the mixer to reduce the mixer NF. In this work, we increased the mixer dc current further to achieve sufficient mixer output power. This leads to significant reduction of the area and a much simpler design compared to other SAW-less transmitters.

II. DA-Less Architecture

As was discussed in Section I, the primary motivation for eliminating the DA arises from the goal of reducing the transmitter noise of a CDMA transmitter in the absence of an off-chip SAW-filter. However, this approach brings several other advantages. The fully differential circuit delivers power to a higher load impedance than a conventional transmitter architecture, where the power is generated in single-ended DA's.

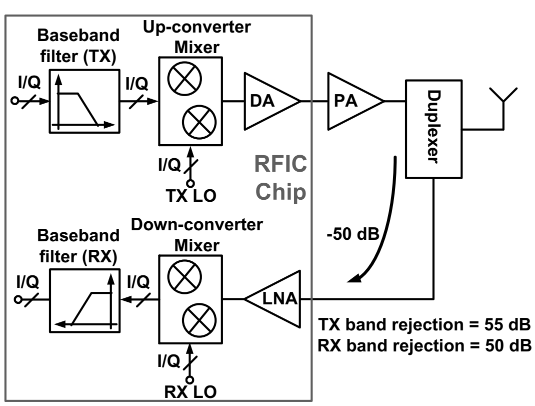


Fig. 1. Block diagram of a typical CDMA transceiver.

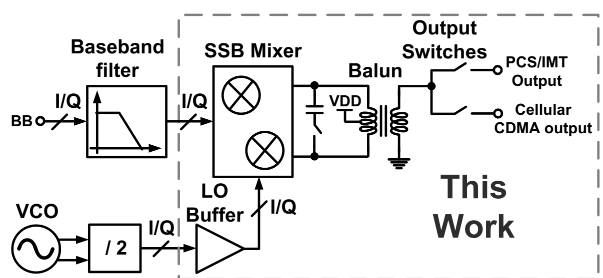


Fig. 2. Simplified block diagram of the DA-less dual-band up-converter.

The block diagram of the proposed DA-less transmitter is shown in Fig. 2. The up-converter uses an on-chip balun for differential to single-ended conversion and the secondary of the balun goes to the output pads via switches. System design considerations require that the up-converter deliver a maximum output power of +4 dBm. Considering the losses in the system (the loss of the balun and output switches), the mixer must generate a maximum power of +10 dBm in the primary side of the balun. Circuit implementation of the DA-less transmitter is discussed in the next section.

III. Circuit Design

The mixer needs to generate +10 dBm output power (referred to the primary of the balun). However, losses in the system lead to an increase in the required signal current to generate the desired output power. This leads to larger output devices and an increase in the power dissipation. Therefore, an architecture is required that maximizes the achievable voltage swing.

A. Up-Converter Topology

Figure 3(a) shows a Gilbert cell mixer and Fig. 3(b) shows a switched-transconductance mixer [6]. Both mixers use cascode (transistors $M7$ and $M8$) to increase the output impedance of the mixer core, and also to protect the mixer core against voltage breakdown.

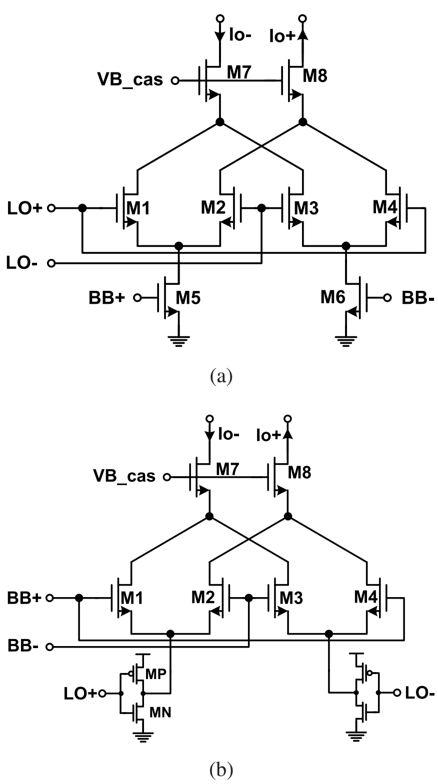


Fig. 3. (a) Gilbert cell based mixer, (b) switched-transconductance mixer.

To compare these two mixers, consider the single-ended stack of the transistors in the mixers of Fig. 3(a) and Fig. 3(b). Both mixers consist of three stacked transistors, but since the LO switch in the switched-transconductance mixer is implemented using a CMOS inverter (transistors MN and MP), it requires a smaller voltage drop across it. Moreover this voltage drop can be reduced to less than 100 mV by proper sizing of the transistor MN (Fig. 3(b)). As a result, the switched-transconductance mixer can achieve a larger voltage swing compared to the Gilbert cell. This difference becomes very important at 1.3 V or lower supply voltages. In addition, as shown in [6], a switched-transconductance mixer can achieve a similar conversion gain and a slightly better NF compared to a Gilbert cell mixer.

The best architecture for power generation at low supply voltages minimizes the number of the transistors in the stack. The switched-transconductance mixer minimizes the effective number of stacked transistors in the mixer. The mixer core is cascoded using a pair of thick-oxide transistors ($M7$ and $M8$) to protect it during the peak of the voltage swing. These cascode transistors improve the achievable Q of the mixer by raising the output impedance. In addition, they can be reconfigured to provide some gain control, as will be shown in Section IV.

B. Output Switch

As shown in Fig. 2, the secondary of the balun is connected to the off-chip power amplifiers via output switches. The output switches must provide low insertion loss, low distortion, and high off-mode isolation. The output switches may also need to provide some gain control to meet the dynamic range requirement.

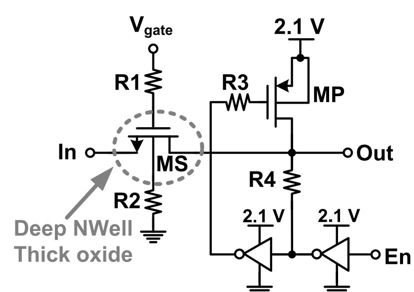


Fig. 4. Simplified schematic of one of the output switches used at the secondary of the balun.

In this work, a floating switch [7] using a thick-oxide deep N-well NMOS switch is used. The simplified schematic of the output switch is shown in Fig. 4 where MS is the switch transistor and resistors $R1 - R4$ are chosen large enough to reduce their noise contribution to the output noise. The floating gate in the switch helps to keep the switch on-resistance roughly constant and independent of the input signal level. At the same time, it prevents gate-oxide breakdown during a negative signal swing. The floating bulk protects the drain-bulk and drain-source junctions against voltage breakdown.

When the switch in on (En is 2.1 V), V_{gate} is connected to 2.1 V and V_{gate} is 0 when the switch is off (En is 0). All the control signals in the output switch use a 2.1 V supply to reduce the on-resistance of the switch, and also for a more robust operation.

Since the DC voltage level at the secondary side of the balun (input to the output switch) is zero, and also to avoid adding extra parasitic capacitance to the load of the balun the input of the switch is DC coupled to the balun. In this case, the drain of MS is connected to ground, via resistor $R4$, during the on mode to reduce the on-resistance. When the switch is off, this node is connected to the 2.1 V supply to achieve better off-isolation. Simulations show that the output switch exhibits 0.5 dB insertion loss and it does not provide significant contribution to the output noise.

IV. Gain Control

In any conventional transmitter, a major portion of the gain control is performed in the DA. However, in a DA-less architecture this gain control must be distributed over the existing blocks shown in Fig. 2. In this case, like most other CDMA transmitters, some portion of the gain control is performed in the baseband filter. The rest of the gain control is done in the mixer core, in the cascode transistors, and in the output switch. These together allow the transmitter to achieve the full dynamic range required for CDMA.

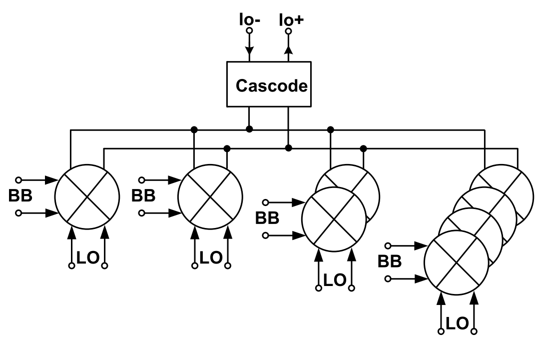


Fig. 5. Gain control mechanism embedded inside the mixer.

In order to insert gain control into the mixer core, it is segmented into different sub-mixers with binary weights [8]. Figure 5 shows the simplified schematic of half of the SSB mixer. The mixer consists of two unit-sized segments, one segment with two unit cells, and one segment with four unit cells. This segmentation brings the ability to control the gain of the mixer with 6 dB steps, and together it covers 18 dB of gain control range. Finer steps for gain control can be achieved using the cascode gain control.

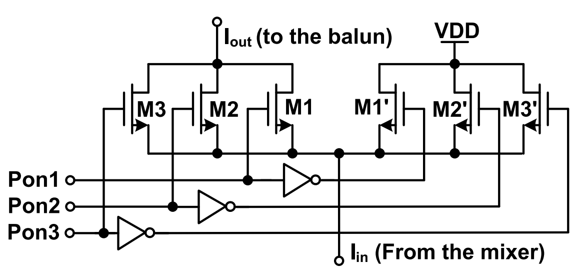


Fig. 6. Implementation of gain control in the cascode.

Cascode gain control is done by sending some portion of the mixer output current to the balun and diverting the rest to the supply. A simplified version of this scheme is shown in Fig. 6 where the transistors are sized to achieve the required gain control steps. Each pair of transistors, ($M1$, $M1'$), ($M2$, $M2'$), and ($M3$, $M3'$), have the same size, and by proper use of the control signals, $Pon1$, $Pon2$, and $Pon3$ in Fig. 6, we can send the output current to the balun or to the supply. However, implementing the entire cascode using the scheme shown in Fig. 6 will double the area required to implement the cascode, and hence it will reduce the conversion gain of the mixer by adding a large parasitic capacitor to the source of the cascode.

Therefore, in the final implementation, the cascode consists of one fixed part and one segmented part, and only one quarter of the cascode is implemented using the segmented architecture shown in Fig. 6. Both parts of the cascode can be controlled independently. The segmented part is used to add fine gain steps during the high gain setting. It can also be used to achieve minimum gain setting when all other gain control settings in the system are set to their minimum values and the fixed part of the cascode is powered down.

Finally, some portion of the gain control is embedded in the output switch. This is only used when all other gain settings in the transmitter are set to their lowest values. Therefore, the switch gain control does not degrade the linearity of the transmitter and provides 10 dB of gain control range.

V. Measurement Results

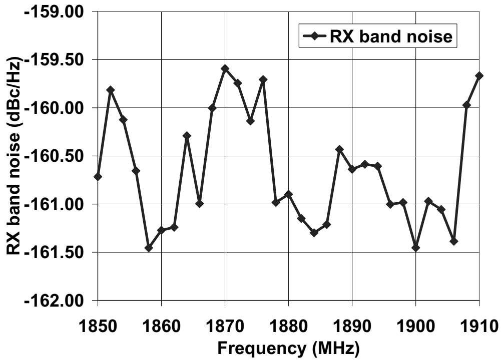
Figure 7 shows the measured receive band noise of the SAW-less DA-less transmitter. The receive band noise for PCS/IMT (at 80 MHz offset) and for cellular CDMA (at 45 MHz offset), vs. frequency, are shown in Fig. 7(a) and Fig. 7(b) respectively. In both cases, the receive band noise is always better than -159 dBc/Hz.

The transmit mask for PCS/IMT and cellular CDMA at +5 dBm output power are respectively shown in Fig. 8(a) and Fig.8(b). As is shown in these figures, the DA-less transmitter meets the ACPR requirement for both modes of operation.

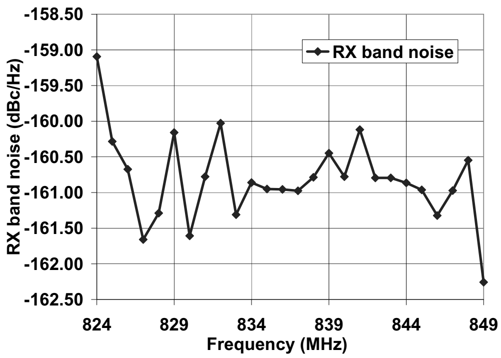
TABLE I
Summary of the performance metrics of the DA-less up-converter.

	PCS/IMT	Cellular CDMA
Max. output power	+5.1 dBm	+4.6 dBm
Min. output power	-75.5 dBm	-67 dBm
Receive band noise	-159.5 dBc/Hz @ 80 MHz offset	-159 dBc/Hz @ 45 MHz offset
ACPR	-45.5 dBc/30 kHz	-48.5 dBc/30 kHz
LO-leakage (at max. power)	-42 dBm	-99.5 dBm
LO leakage (at min. power)	-99.4 dBm	-79.8 dBm
Image suppression	-31 dBc	-37.8 dBc
Current consumption (at peak output power)	180 mA	150 mA

Table I summarizes the measured results of the DA-less transmitter. The up-converter uses a single 1.3 V supply when operating in cellular band and uses a 1.5 V supply for PCS/IMT. The current consumption for cellular band is dominated by the up-converter current because of the low Q of

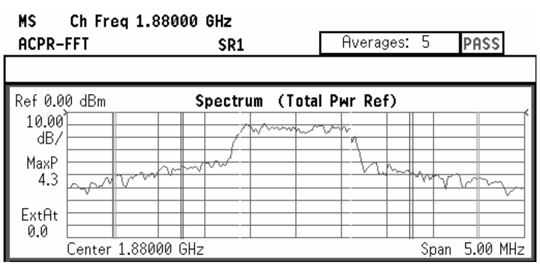


(a)

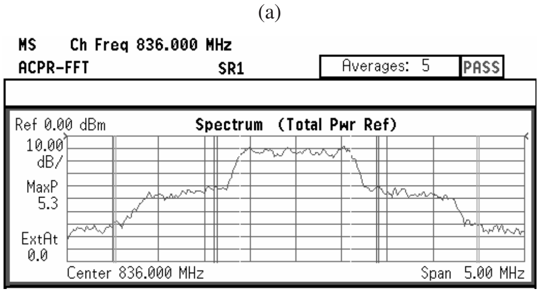


(b)

Fig. 7. Measured RX band noise for (a) PCS/IMT, and (b) cellular CDMA.



(a)



(b)

Fig. 8. Measured transmit mask and ACPR for (a) PCS/IMT, and (b) cellular CDMA.

the balun in this band. In PCS/IMT, the current consumption of the LO buffers is much larger. The chip is packaged using flip-chip technology. Figure 9 shows the chip microphotograph. The core area of the up-converter is 1.0 mm^2.

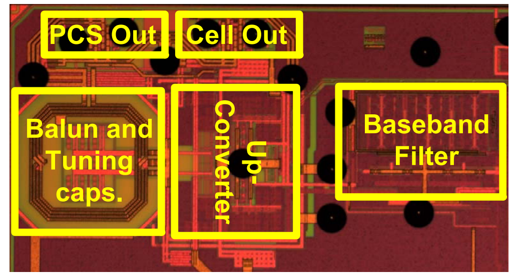


Fig. 9. Chip microphotograph.

VI. Conclusions

This work presented a new approach to removing the off-chip SAW filter from the CDMA transmitter by removing the driver amplifiers (DA's). Removing the DA's provides for a very low receive band noise, better than -159 dBc/Hz, without using complicated noise canceling methods. The mixer delivers up to +5 dBm output power to the off-chip PA's. The current consumption at peak output power is increased due to the limited Q of the on-chip balun. The embedded gain control mechanism in the baseband filter, mixer core, cascode, and the output switches allows the transmitter to achieve the full dynamic range required by CDMA. Removing the DA's, along with integrating the tuning capacitors inside the balun coil, helped to reduce the silicon area to 1.0 mm^2. The required PCB area is also reduced since no external matching component or SAW filter is required for this chip.

Acknowledgments

The authors would like to thank Dr. Prasad Gudem of Qualcomm for supporting this project, and Mr. Khahn Dinh for help with the layout.

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