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A Fast Settling, High DC Gain, Low Power OPAMP Design for High Resolution, High Speed A/D Converters

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Abstract— **A fast settling, low power, high dynamic range OPAMP with a DC gain of 96 dB has been designed. Simulations have been performed in 0.35μm CMOS technology for slow, nominal and fast models. High DC gain has been achieved by adding gain boosting active blocks to the main OPAMP. In this design, a telescopic OTA has been chosen as the main opamp due to its fast settling and low power advantages, as well as the gain boosting OPAMPs. Transient simulation indicates a settling time of 17ns for a global feedback with β=1/2. Although telescopic OPAMPs suffer from inherent low output voltage swing, a dynamic range of 83 dB has been achieved in this design. A power consumption of 4.1mW is obtained for the total circuit including the main OPAMP, gain boosters and the bias circuitry.**

Index Terms—**fast settling, gain boosting, high DC gain, telescopic configuration**

I. INTRODUCTION

Designing high performance analog circuits is becoming more challenging as transistors are scaled to smaller dimensions and power supplies are reduced to lower levels. Operational amplifier (OPAMP) is the main component of an analog circuit and has a crucial role in the circuit performance, so all the challenges of analog circuit design are directly translated into an inquiry for high performance OPAMPs. The performance of the switched-capacitor circuits and analog to digital (A/D) converters can be significantly degraded due to OPAMP non-idealities such as finite DC gain, finite bandwidth and slow settling. Achieving high-resolution A/D converters requires OPAMPs with high DC gain [1]. In addition, the main specifications of a switched-capacitor filter such as the transfer-function, resonant frequency and quality factor are affected by the finite DC gain and bandwidth of the OPAMPs [2]. Although some solutions have been proposed to effectively reduce the repercussion of such non-idealities, designing fast settling OPAMPs with high DC gains is still indispensable for many applications [3].

A feasible configuration, suitable for high-speed circuits and moderate DC gain applications, is a stacked structure such as a telescopic or folded-cascode [4]. These structures guarantee a considerable improvement in speed and output impedance for a given level of power consumption in comparison with a simple two-stage amplifier. However, the DC gain of a stacked structure is too low for high accuracy applications such as high-resolution A/D converters and switched-capacitor resonators. Cascading the stacked OPAMPs in a multistage configuration may significantly improve the DC gain [5], but at the expense of higher power consumption and drastically reduced speed. A promising gain boosting technique is to insert an active feedback path from the output of the gain stage in order to increase both the DC gain and the output impedance [6-8] (Fig.1). Both the DC gain and the output impedance of the main OPAMP are multiplied by a factor of about $(1+A_0)$, where A_0 is the gain of the additional feedback path. It has been demonstrated that this additional gain booster has almost no degrading effect on the unity gain bandwidth (UGBW) and thus the speed of the main amplifier, provided that the UGBW of the additional OPAMP is chosen properly [9]. The additional OPAMP creates a doublet in the frequency response of the total gain-stage, which should be set to occur at a reasonably higher frequency than the UGBW of the main amplifier, in order to avoid abnormal transient behaviors. The important privilege of this approach is that the additional OPAMP need not be a very well designed fast-settling high DC-gain OPAMP as the main amplifier, so it does not add so much to the total power consumption or parasitic capacitors, as well as the labor work

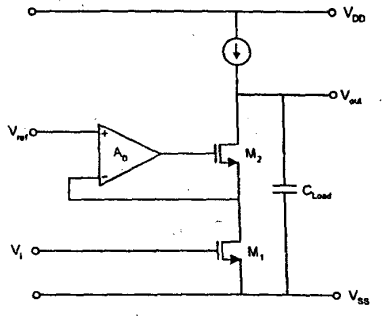

Fig.1. Schematic of a gain-enhanced configuration. The OPAMP with DC gain, A_0, is added to the main cascode OTA for gain boosting.

that might be required to design a new OPAMP.

In this paper, we present an OPAMP design, which combines the high-speed and low-power advantages of the telescopic configuration with the privilege of the gain boosting technique, in order to realize a fast settling OPAMP with high DC gain. Telescopic configuration is also chosen for the gain boosting OPAMPs due to its low power and high-speed profits. This design presents superior specifications in comparison with a previous work manipulating folded-cascode gain-boosting stages [9]. Advantages of high DC gain and fast settling, makes this design a proper candidate for applications in which high speed and high resolution are required.

II. THE OPAMP STRUCTURE

The proposed gain-enhanced configuration is shown in Fig. 2. The main OPAMP is a telescopic OTA with NMOS input transistors, which is a promising choice for a fast settling OPAMP. Although a telescopic OTA has a low output swing in comparison with similar structures such as folded-cascode, exploiting a fully differential structure accompanied with proper design of a low noise telescopic OTA, puts forth the chance of realizing an OPAMP with a high dynamic range. The low output voltage swing may be alleviated by choosing a relatively high aspect ratio for the tail transistor, M_9. The degrading effects of clock feedthrough and common mode distortions are significantly reduced by using fully differential structures . The only drawback of a fully differential structure is the need for a common-mode feedback circuit to set the common-mode output voltage of the output terminals and prevent the possible drift in the DC bias of the transistors. The gain boosting OPAMPs OP_1 and OP_2 are fully differential telescopic OTAs with NMOS and PMOS input transistors, respectively. For the same reasons, additional common-mode feedback circuits are also required for the gain boosting OPAMPs.

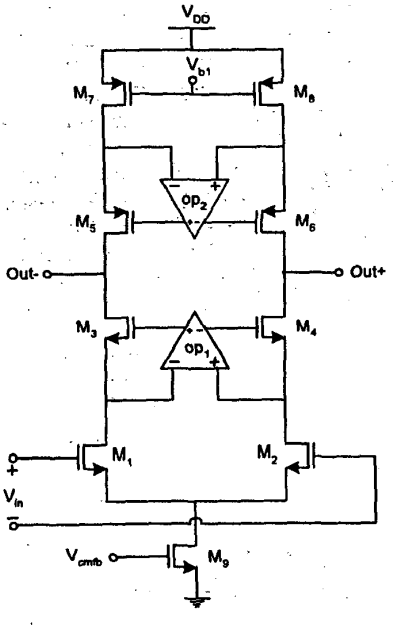

Fig.2. The schematic of the proposed fully differential gain-enhanced OPAMP. The gain boosting OPAMPs OP1 and OP2 are fully differential telescopic OTAs with NMOS and PMOS input transistors, respectively.

The common-mode feedback circuits used for this design are all switched-capacitor structures. Switched-capacitor structures are generally preferred for common-mode feedback circuits due to their high accuracy and high linearity in comparison with continuous-time structures. The schematic of the switched-capacitor common-mode feedback is depicted in Fig.3. It should be mentioned that the value of the capacitor C_{S2} should be considerably larger than the total parasitic capacitance of the output nodes, in order to guarantee a reasonable common-mode gain. On the other hand, this capacitor adds to the output load and reduces the operation speed of the OPAMP. Therefore, an intermediate value should be chosen for C_{S2}.

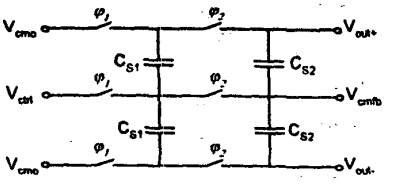

Fig.3. Schematic of the switched-capacitor common-mode feedback structure exploited in this design.

III. SIMULATION AND RESULTS

Simulations have been performed in 0.35μm CMOS technology, for nominal, slow and fast models. A power supply of 3 volt has been used for this technology. A DC gain of 96 dB and a phase margin of 77° were obtained through AC analysis for fast model and the relevant bode diagram is given in Fig.4. In order to assure a well-behaved transient

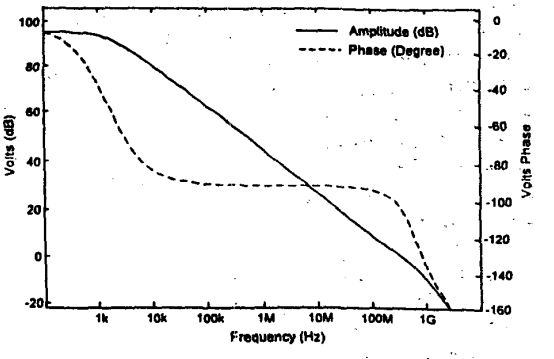

Fig.4. The bode diagram of the AC analysis. A DC gain of 96dB and a phase margin of 77° is obtained for fast model.

response, the doublet created by the additional OPAMPs should be set at frequencies reasonably higher than the unity gain frequency of the main OPAMP. Furthermore, for stability reasons, the unity gain frequency of the additional OPAMPs should be set at frequencies lower than the second pole of the main OPAMP[9]. As observed in Fig.4, the doublet is placed well above the unity gain frequency of the main OPAMP and therefore it will not corrupt the transient response.

The transient behavior has been simulated by placing the OPAMP in a gain-stage circuit to provide a global feedback with a factor of β=1/2, as shown in Fig.5(a). Simulating with slow model results in a settling time of 17ns corresponding to 0.01% settling accuracy. The transient response is depicted in Fig.5(b).

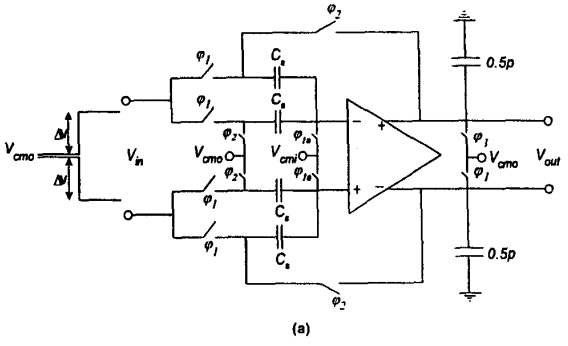

Fig.5. (a) The gain-stage circuit used for transient simulation. (b) The transient response obtained by simulation of the gain stage circuit.

In order to evaluate the dynamic range of the OPAMP, the circuit in Fig.6 has been used for simulation. The rms value of the output noise has been obtained by AC simulation of this circuit. The output swing of the OPAMP has been estimated by applying a sinusoidal signal to the input and determining the maximum amplitude of the input sinusoidal that does not result in a distorted output signal. The first harmonic of a non-distorted signal is assumed to be at least 85dB stronger than the other harmonics, as verified by fast Fourier transform (FFT). A dynamic range of 83dB is achieved for slow model. The C_S capacitors in this circuit have the same values as those in the gain stage circuit of Fig.5(a). As the capacitor size increases, the output noise is reduced, but on the other hand the transient response becomes too slow. Therefore, a compromise between the dynamic range and speed would determine the size of the capacitors.

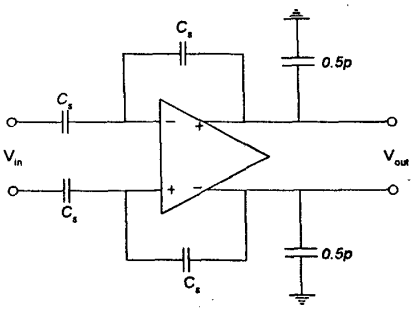

Fig.6. The structure used for dynamic range evaluation.

The power consumption of the total circuit, including the main OPAMP, gain boosters and the bias circuitry is obtained as 4.1mW in fast model. The simulation results of this section are summarized in table I.

	Slow	Nominal	Fast
DC Gain (dB)	105	100	96
Settling time (ns)	17.0	15.5	14.2
Dynamic Range (dB)	83.0	82.6	82.1
Total Power Consumption (mW)	3.9	4.0	4.1

Table I- The summary of specifications and simulation results.

IV. CONCOLUSION

In this paper, we have presented the design of a fast settling, low power OPAMP with a high DC gain. The fast settling privilege of the telescopic OTAs has been combined with the gain boosting technique to realize an OPAMP with a settling time of 16ns and a DC gain of 96 dB. Proper design of the low-noise OPAMP in addition to exploiting a fully differential structure led to a dynamic range of 83dB, in spite of the inherent swing limitation in the output of telescopic structures. Simulation shows a power consumption of 4.1mW for the total structure. This design is very promising for high resolution, high-speed switched-capacitor applications.

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