A Modified Deadbeat Control for Single-phase Voltage-source PWM Inverters Based on Asymmetric Regular Sample*

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***Abstract*-This paper proposed a new digital multiple feedback control for uninterruptible power supply (UPS) with single-phase half-bridge inverter. The control scheme is based on sensing the voltage of the filter's capacitor and load current. And a state observer is used to predict the capacitor current. Thus current deadbeat control can be achieved, which is easy to be deduced by discrete state equation of the LC filter. Then an outer voltage feedback loop is also used to ensure load voltage to be sinusoidal and well regulated. It is shown the control scheme which is simple and can be designed easily offers improved performance over the traditional deadbeat control especially with nonlinear load. Simulation and experimental results based on TMS320F240 (DSP) proved it.**

I. INTRODUCTION

UPS are used to interface critical loads such as computers and communication system to the utility system. The output voltage of the UPS inverters is required to be sinusoidal with minimum total harmonic distortion. SPWM scheme, which is used to depress low order harmonics, is the most important way to achieve "clean" sinusoidal waveform. However, this scheme including optimum PWM scheme to eliminate harmonics can't suppress the distortion under nonlinear loads.

To over this drawback, many control strategies are proposed such as PID control, instantaneous feedback control, sliding mode control, repetitive control and so on [1][2]. It is difficult to have both excellent transient response and low THD of output waveform because the waveform is influenced by many facts:

(1). The load is changeable especially nonlinear load that causes intense current disturbance.

(2). SPWM modulation is not an ideal amplification including dead-time and conducting resistance of device.

With the development of microprocessor and digital signal processor (DSP), the control scheme is demanded to be numeric because of its high reliability, coincidence and flexibility. But it is difficult to transform analog control into digital control because of the limit of sampling frequency and time lag of calculation.

Deadbeat control is applied into power electronics in the middle 1980's [3]. It is a digital control method with fast response and precise tracking reference with linear load by real time calculating the pulse width of the next switch period at each sample time. Then deadbeat control with load disturbance observer is proposed which in some distance solved the waveform distortion with capacitor feed rectifier [4]. But this scheme demanded relatively large filter capacitor to compensate the error between predicted load current and real load current.

A new control scheme with multiple state feedback has been proposed [5]. In this technique the current in the filter capacitor is used as the feedback variable to achieve sinusoidal capacitor current. An outer voltage current loop is also used for load voltage regulation and compensation for perfection in the implementation of current control loop. But it is a kind of analog control. In order to achieve digital multiple feedback, a robust digital control was proposed [6]. Though there are excellent experimental result shown in this paper, it is a little complex to achieve the algorithm because the system design is a little complex and two observers is to

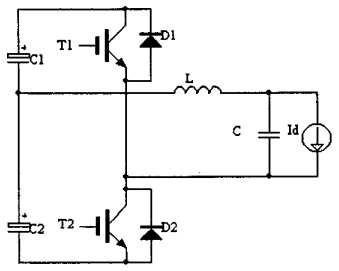

Fig. 1 Circuit of the single-phase half-bridge inverter

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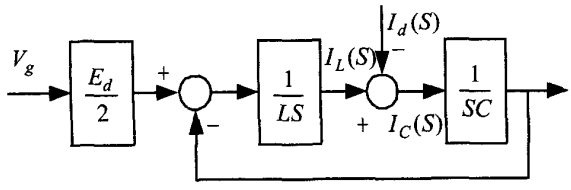


Fig. 2 Model of half-bridge single-phase inverter

be accomplished.

This paper proposed a new algorithm of digital multiple feedback control that is simple and can be designed easily. The inner loop is achieved by deadbeat control that is easy to be deduced by discrete state equation. In order to improve system response, asymmetric regular sample is adopted that means the sample frequency is as high as two times switching frequency. To compensate the time lag of A/D conversion and calculation, state observer is used to predict the capacitor voltage and induction current of the next sample. The outer loop can adopt a proportional compensator because of the fast response of the inner loop.

Theoretical analysis and experiments show the validity of the proposed method. The scheme is implemented by TMS320F240 (DSP) with the A/D sampling frequency is 40kHz as high as two times the PWM carrier frequency.

II. The Proposed Control System

A. Inverter Math Model for Asymmetric Regular Sample

Fig.1 shows the circuit of the single-phase half-bridge voltage source UPS inverter. It mainly consists of inverter-bridge, output filter and load. If the load current I_d is regarded as step disturbance and the deadtime is neglected with the equivalent resistive of the inductor and capacitor. Fig.2 shows the model in continuous domain. The ideal system state equation is:

$$\begin{cases} \begin{bmatrix} \dot{V}_C \\ \dot{I}_L \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{C} \\ -\frac{1}{L} & 0 \end{bmatrix} \begin{bmatrix} V_C \\ I_C \end{bmatrix} + \begin{bmatrix} 0 & -\frac{1}{C} \\ \frac{1}{L} & 0 \end{bmatrix} \begin{bmatrix} V_i \\ I_d \end{bmatrix} \\ y = [1,0]\mathbf{x} \end{cases} \quad (1)$$

V_i is the inverter bridge output. To a half bridge inverter (Fig.1), V_{in} has only two values: +E or –E. The discrete-time system equation of two-lever switching pattern shown in fig.2 can be deduced by (2) in [7].

$$\mathbf{x}(t) = e^{A(t-t_0)}\mathbf{x}(t_0) + \int_{t_0}^{t} e^{A(t-\tau)} Bud\tau \quad (2)$$

Thus the discrete state equation from t_{01} to t_{03} is:

$$\mathbf{X}(k+1) = \Phi X(k) - \mathbf{G} * \Delta T + \mathbf{H} + \mathbf{F} I_d \quad (3)$$

Where:

$$\begin{cases} \Phi = e^{\mathbf{A}T} = \begin{bmatrix} \Phi_{11} & \Phi_{12} \\ \Phi_{21} & \Phi_{22} \end{bmatrix} \\ \mathbf{G} = \begin{bmatrix} 0 \\ 1/L \end{bmatrix} E_d = \begin{bmatrix} 0 \\ g \end{bmatrix} \\ \mathbf{H} = \mathbf{A}^{-1}(e^{\mathbf{A}T} - \mathbf{I}) \begin{bmatrix} 0 \\ 1/L \end{bmatrix} \frac{E_d}{2} = \begin{bmatrix} h_1 \\ h_2 \end{bmatrix} \\ \mathbf{F} = \mathbf{A}^{-1}(e^{\mathbf{A}T} - \mathbf{I}) \begin{bmatrix} -\frac{1}{C} \\ 0 \end{bmatrix} \end{cases} \quad (4)$$

T is the half of the PWM carrier period and $\Delta T = t_{03} - t_{02}$.

Equation (4) is corresponding to the former half PWM carrier of the two-lever PWM pattern shown in fig.2. According to average state space method, the same equation can be got for the latter half PWM carrier except $\Delta T = t_{12} - t_{11}$.

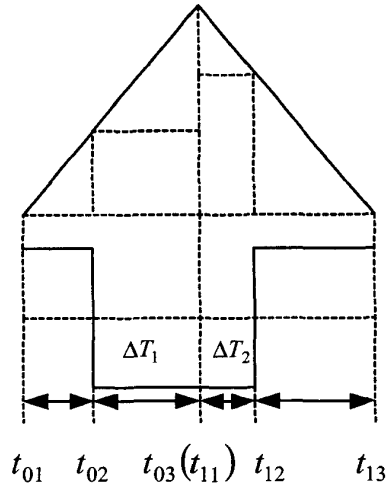


Fig. 3 Two-level PWM pattern of asymmetric regular sample in a PWM carrier

B. Deadbeat Control for Capacitor Current

According to (3), the current deadbeat control is achieved as follow:

$$\Delta T = \frac{I_C^*(k+1) - \Phi_{21} V_C(k) - \Phi_{22} I_C(k) - h_2}{g_2} \quad (5)$$

Where: $I_C = I_L - I_d$ and $I_C^*(k+1)$ is the current given.

Equation (4) means that $I_C(k)$ lags $I_C^*(k+1)$ by one sampling time, so that the filter's capacitor current track the reference sinusoidal current, which means that the inner loop has fast response. Fig.3 shows the inner loop block diagram.

It is well known that:

$$v_c(t) = v_c(t_0) + \frac{1}{C}\int_{t_0}^{t} i_c dt \tag{6}$$

That is to say, the capacitor voltage is related not only to the capacitor current, but also the initial value of the capacitor current. Because it is impossible to get precise sinusoidal capacitor current, equation (5) is insufficient for the output voltage control. The outer voltage loop is essential.

C. The Outer Voltage Loop

The function of the outer voltage loop is to compensate the voltage error of the period before.

The error may be caused by the following reason:

1) It is difficult to attain precise value of the parameter L and C.

2) I_d is regard as step disturbance that causes sample error especially the load is rectifier with large capacitor leading intense current change.

That is to say, the outer loop should have the ability to suppress the model error and it has the ability to improve the system robustness. Generally speaking, simple proportion adjuster can be adopted to compensate the voltage error because the sample and calculation time lag influences on the control performances can be neglected in the system for the sample frequency is high enough.

So, the control algorithm is:

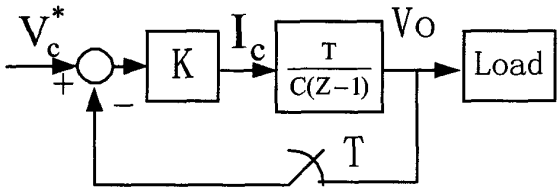


Fig. 5 The equivalent outer loop

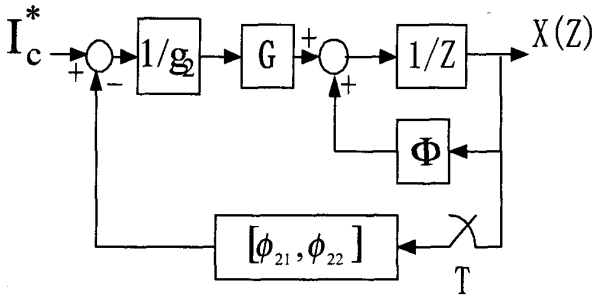


Fig.4 The discrete system block diagram

$$\Delta T = \frac{K(V_C^*(k) - V_C(k)) + I_C^*(k+1) - \Phi_{21}V_C(k) - \Phi_{22}I_C(k) - h_2}{g_2} \tag{7}$$

D. State Predict by State-observer

In order to compensate the time lag, state observer is used to predict the next sample time state value shown in Fig.6 according to (8). As is known that the time lag is mainly caused by A/D sample delay and computational time of DSP that can be easy drew from fig.3. At time t_{01}, V_c and I_L must first be sampled, then ΔT_1 is calculated.

$$\mathbf{X}_p(k+1) = (\Phi - \mathbf{LC})X_p(k) - \mathbf{G}*\Delta T + \mathbf{H} + \mathbf{F}I_d + LCV_c(k) \tag{8}$$

Where:

$$X_p(k) = \begin{bmatrix} V_{cp}(k) & I_{Lp}(k) \end{bmatrix}^T$$

Then:

$$\Delta T = \frac{K_p + I_C^*(k+1) - \Phi_{21}V_{Cp}(k) - \Phi_{22}I_{Cp}(k) - h_2}{g_2} \tag{9}$$

Where:

$$K_p = K(V_C^*(k) - V_C(k))$$

From (8) and (9), one sample ahead preview (OSAP) can be achieved. At time t_{01}, $V_c(t_{01})$ and $I_L(t_{01})$ must first be sampled, then is $V_c(t_{11})$ and $I_L(t_{11})$ can be calculated by (8). At last ΔT_2 can be calculated by (9).

III. System Stability And Transient Response

It is well known that the condition of discrete system stability is that all the poles must be in unit circle. In order to

simply the system, the inner loop is first analyzed.

The inner loop transfer function is:

$$\frac{X(Z)}{I_C^*(Z)} = [Z\mathbf{I} - \Phi + \mathbf{G}[\Phi_{21} \quad \Phi_{22}]/g_2]^{-1}\begin{bmatrix}\frac{g_1}{g_2}\\ 1\end{bmatrix}$$

$$= \begin{bmatrix} Z-\Phi_{11}+\frac{g_1}{g_2}\Phi_{21} & -\Phi_{12}+\frac{g_1}{g_2}\Phi_{22} \\ 0 & Z \end{bmatrix}^{-1}\begin{bmatrix}\frac{g_1}{g_2}\\ 1\end{bmatrix} \tag{6}$$

Then:

$$\frac{I_C(Z)}{I_C^*(Z)} = \frac{X_2(Z)}{I_c^*(Z)} = \frac{Z-\Phi_{11}+g_1\Phi_{21}/g_2}{Z(Z-\Phi_{11}+g_1\Phi_{21}/g_2)} = \frac{1}{Z} \tag{7}$$

From (7), the inner state feedback law achieves pole-zero cancellation and the other pole is at the origin of Z-plane. So the actual capacitor current is lagging reference with one sampling time.

Therefore, the inner loop can be simplified the equivalent system block diagram is shown in fig.5. Then the transfer function is:

$$G(Z) = \frac{\frac{KT}{C(Z-1)}}{1+\frac{KT}{C(Z-1)}} = \frac{KT/C}{Z-1+KT/C} \tag{8}$$

Obviously, $|Z|<1$ is the condition for stability.

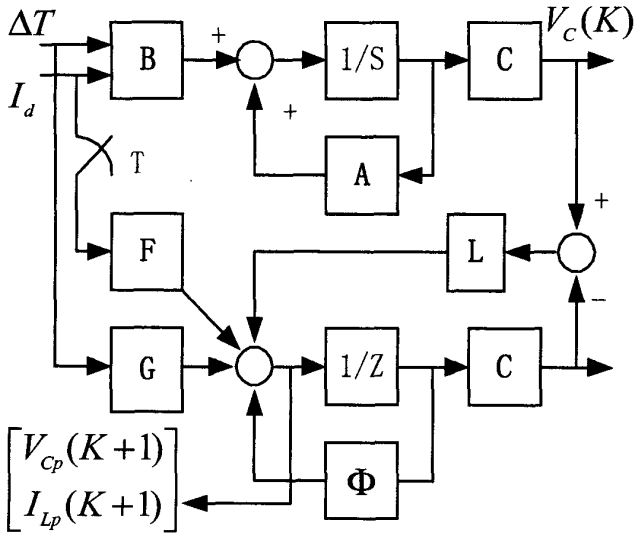


Fig. 6 State observer based on discrete state-equation

If $K = \frac{C}{T}$, then $G(Z) = \frac{1}{Z}$. That is to say, the voltage deadbeat control will be achieved. But actually, the precise system model is difficult to attain and the delay of disturbance detection is inevitable. On the other hand, the value of K will

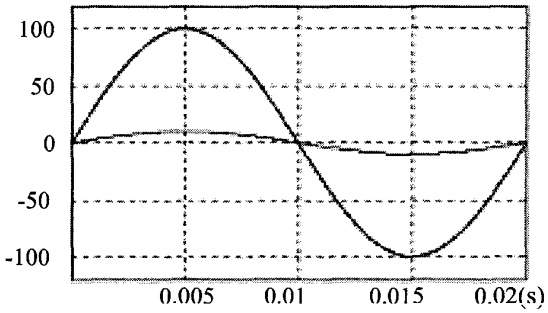


Fig.7 Simulation waveform of the output voltage and current with resistive load (R=10 Ω)

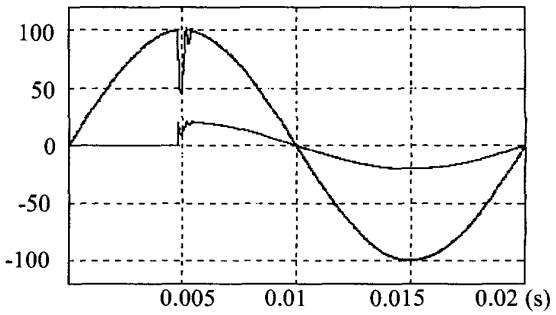


Fig. 8 Simulation waveform of the output voltage and current with sudden step load (R= ∞ → 5Ω)

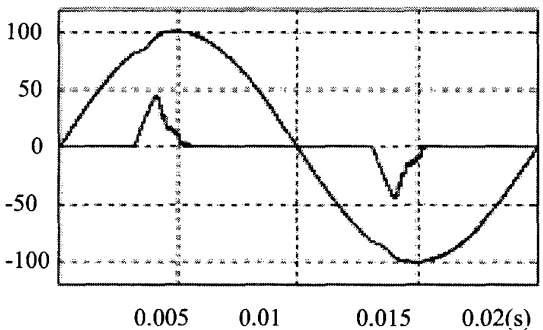


Fig. 9 The output voltage and current waveform feeding with capacitor-resistive rectifier

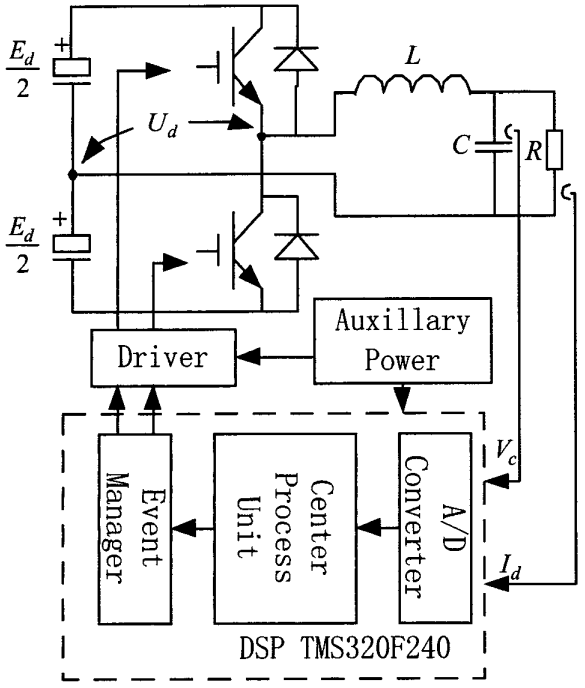
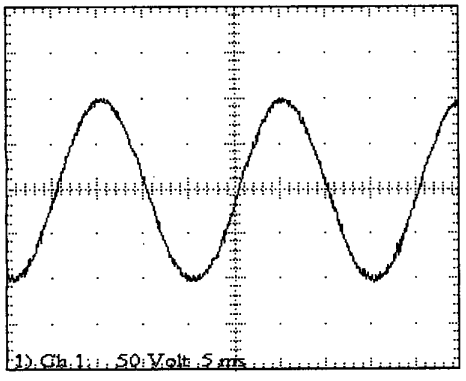


Fig.10 the system construction



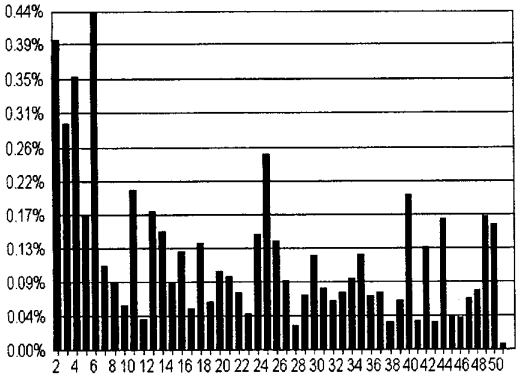
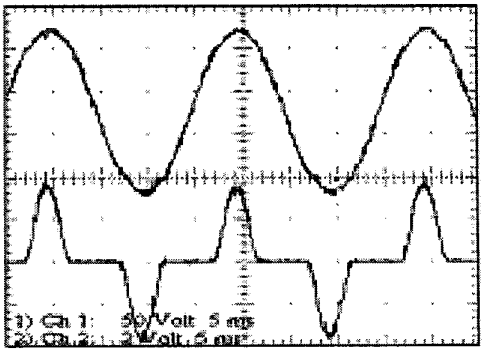


Fig.11 Output voltage waveform and harmonic magnitude of the fundamental amplitude



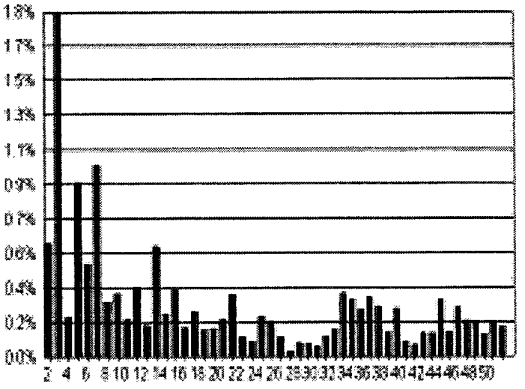


Fig.12 Output voltage and current waveform with rectifier load and voltage harmonic magnitude of the fundamental amplitude (current: 10A/div)

influence the system stability and output precision. Because there is no any disturbances that have been suppressed by current control loop, it is unnecessary to achieve voltage deadbeat control as a rule.

IV. Simulation And Experimental Result

Computer simulation of the half-bridge inverter system controlled by the modified deadbeat control algorithm is carried out to study the output characteristics. The parameter of the circuit is:

A/D sampling period=T=25uS

Switching period =2T=50uS

Reference sinusoidal wave =50Hz, 100V (peak)

DC bus voltage=300V

Filter inductor L=1mH

Filter capacitor C=20u

Rated load resistance=5 Ω

MATLAB/Simulink verifies operation of the proposed control strategy with ideal model by time-domain simulation. Fig.7, fig.8 and fig.9 show the simulation output waveform of

voltage and current under resistive load, sudden step load and capacitor with large capacitor respectively. The THD of the voltage in fig.6 and fig.8 is 0.2% and 1.26% respectively.

TMS320F240 has the architecture features necessary for high-speed signal processing and digital control functions, and it has the peripherals to provide a single-chip solution for motor control and inverters. Here, it is used to achieve the proposed control scheme.

Fig.10 shows the construction of the experimental main circuit and the digital controller based on Fig.4, Fig.5 and Fig.6.

Fig.11 shows the output voltage waveform with no load and its THD=1.11%. Fig.12 shows the output voltage and current waveform with rectifier load and voltage THD=2.7%.

The reason that the THD of experiment result is higher than the simulation is:

(1). SPWM modulation is not an ideal amplification including dead-time and conducting resistance of device. But the simulation is achieved under ideal mathematical model.

(2). The precision of TMS320F240's A/D converter is a little lower because it has only 10 bits which means that the outer voltage error proportion can't be too large.

(3). The state observer can also generate error.

V. Conclusion

The deadbeat control PWM VSI can achieve low harmonic distortion in a sinusoidal output waveform in steady-state operation. The transient response of the strategy is very quick. A fast response digital control method for the inverter was presented. The performance of state observer and high sampling frequency obtained by asymmetric regular sample allowed the proposed method to achieve quick and exact current control. The method is fit for full digitalization of small capacity UPS.

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