An MMIC Receiver Front-end Design for 2.4GHz Frequency Band Applications in 0.2μm GaAs Pseudomorphic HEMT Process

Farshad Eshghabadi
Young Researchers Club
Islamic Azad University (IAU)
Science and Research Branch
Tehran, Iran

Massoud Dousti
Dept. of Electrical Engineering
Islamic Azad University (IAU)
Science and Research Branch
Tehran, Iran

Mahdi Yazdizadeh
Dept. of Electrical Engineering
Islamic Azad University (IAU)
Dezful Branch
Dezful, Iran

***Abstract*—A 2.4-GHz radio receiver front-end for ISM-band applications incorporating the superheterodyne architecture is designed and simulated in 0.2μm GaAs pseudomorphic HEMT technology. It features an ultra low-noise cascode-topology highly-integrated amplifier followed by an external image-rejection band-pass filter and an active half-Gilbert-cell down-conversion mixer with an IF frequency of 340 MHz. The receiver chain showed a gain, noise figure and input-referred third-order intercept-point equal to 17.9 dB, 1.8 dB and –18 dBm, respectively. Operating in 3-volt DC supply, it draws a 33-mA current. Finally, the characteristics of this front-end are compared in brief with those of a front-end of the same topology, but in a different process.**

Keywords- MMIC; front-end; LNA, mixer; GaAs; PHEMT

I. INTRODUCTION

Monolithic Microwave integrated circuits (MMICs) for wireless applications market have found much interest owing to their potential low cost and the prospect of system level integration. The needs for low voltage operating RF chips with lesser power consumption and higher performance/price ratio have led to increased interest and research of the front-end receiver. This huge increase in demand on microwave communications has resulted in an effort to provide components and complete systems on an integrated circuit.

The viable IC technology for RF circuits continues to change. Performance, cost, level of integration, and prior successful experience are critical factors in the decisions made by the designers. At present, GaAs and SiGe BiCMOS technologies constitute the major section of the RF market [1].

The year 1985 heralded the era of "band-gap engineering," which is the technique of mixing different semiconductor materials to create transistors with specific solid-state properties. This eventually led to the development of a high-electron-mobility transistor (HEMT) low-noise amplifier (LNA) MMIC in 1988 and a heterojunction bipolar transistor (HBT) power amplifier in 1989 [2].

Other milestones along the MMIC development pathway include the appearance of the launch of Plessey's commercial 0.2μm gate length pseudomorphic HEMT (PHEMT) process in 1996. Silicon germanium (SiGe) transistors are also in resurgence with frequency responses comparable to GaAs [3].

Although super heterodyne architecture is large in size and consumes more power than other architectures, it is chosen because of its high sensitivity and linearity characteristics and strength against noises.

There are many technologies suitable for a 2.4 GHz receiver system. Although Gallium-Arsenide technologies are more costly than silicon-based technologies, but they lend themselves to high integration and offer very low noise transistors.

This work presents RF front-end receiver for 2.4-GHz frequency ISM band designed and optimized in 0.2μm GaAs pseudomorphic high electron mobility transistors (PHEMT) MMIC process.

The front-end comprises a low-noise amplifier (LNA) and a downconversion mixer. A 2.4 GHz cascode-topology LNA with resistive feedback is described, as well as a single-balanced Gilbert-cell type mixer that downconverts the RF (radio frequency) signal to an IF (intermediate frequency) of 340 MHz. The receiver front-end is completed with an external voltage-controlled oscillator (VCO) which provides the local oscillator (LO) signal to the mixer and an external band-pass filter (BPF) which acts as an image-rejection filter. This filter noticeably improves the overall noise figure (NF).

The building blocks have been optimized to be nonsensitive to 5 percents of variations in fabrication; so, they preserve their own specified characteristics such as matching. All the matching components were on-chip excluding DC blocks and the balun inductors.

This paper is organized as follows: in Section 2 front-end components will be explained briefly; In Section 3 the simulation results will be presented, and Section 4 contains the conclusions with a brief comparison with a front-end of the same building blocks in an SiGe BiCMOS process.

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II. FRONT-END COMPONENTS: DESIGN ANALYSIS

The front-end building blocks are an LNA and an active down-conversion mixer. The receiver is completed by an external VCO and BPF (figure 1). The receiver is based on a 340-MHz IF architecture on the basis of analysis of the spurious response and half IF problem. If the IF is too low, the image frequency is too close to the receiver band and too high a selectivity is required in the image rejection filter. If the IF is too high, the number of spurious responses that arise from the frequencies falling within the RF passband increases dramatically [4].

A 0.2µm GaAs PHEMT technology was used for these designs. All the components integrated in this chip should operate at 3-volt single supply voltage

A. LNA

This LNA was designed in a single-ended two-stage cascode-topology with a resistive shunt feedback to achieve high gain and high reverse isolation at low power consumption (figure 1). In addition to noise figure and gain, the stability of LNAs is also of concern. Stern stability factor is defined as:

$$K = \frac{1+\left|\Delta\right|^2-\left|S_{11}\right|^2-\left|S_{22}\right|^2}{2\left|S_{11}\right|\left|S_{22}\right|} \qquad (1)$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$. If $K > 1$ and $\Delta < 1$, then the circuit is unconditionally stable. Equation (1) suggests that stability improves as S_{12} decreases, i.e., as the reverse isolation of the circuit increases [1].

The higher reverse isolation is achieved by avoiding miller effect. This can be done using a cascode topology, but at the cost of a somewhat higher noise figure. The cascode topology has the inherent advantage of separating the output and input optimization criteria in the LNA circuit and also improves S_{12} which helps more attenuation of LO leakages from the mixer to the antenna; This LO-to-RF leakage can cause severe interferences.

This topology is sufficient for a gain in excess of 16.5 dB in the entire band. The input matching is optimized to compromise input reflection (S_{11}) and noise figure (NF). For the used transistors, the optimum noise figure matching point is very close to the conjugate-matching point, so that S_{11} and NF can be optimized simultaneously. In an HBT LNA, The most effective way of improving the NF is increasing area of Q_1 [3], but here it is avoided to have more-than-enough increase in the gate width (figure 2) and gate voltage where using PHEMT transistors gave an NF of 1 dB. As can be seen in figure 2, an increase in gate width to achieve higher linearity and less intermodulation distortion causes an increase in NF and power consumption.

The feedback resistor R_f is chosen on the compromise among the parameters such as NF, gain, input impedance matching and linearity. Use of inductive degeneration (L_S) at the source leads to a wideband match at the input as well as it increases the linearity; but it causes an increase in noise figure. The inductor L_D is used for biasing and loading, and also forms the output matching with L_{out} to 50Ω impedance.

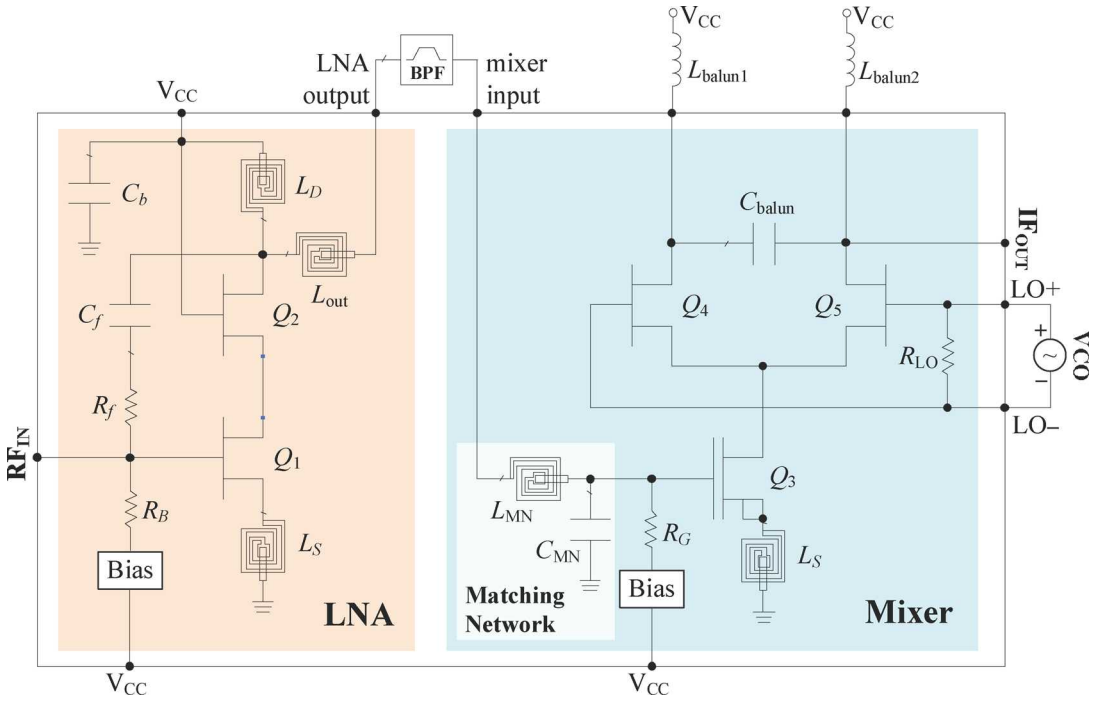

Figure 1. Block diagram of front-end with the schematics of building blocks

The additional resistive shunt feedback circuit helps further match the gain and noise optimum points. The feedback resistance R_f does not increase the NF if it has high value over 1 KΩ [5]. However, in this design R_f is chosen 600 Ω to compromise between the input matching, minimum NF and gain. The area of Q_1 and Q_2 was optimized to acquire high input-referred third-order intercept point (IIP3) (figure 3) and high level of output matching.

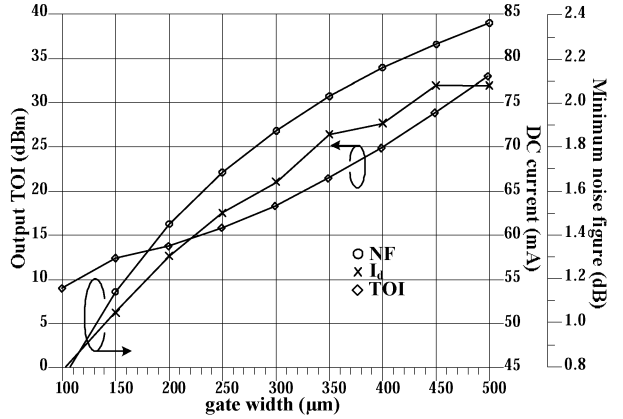

Figure 2. PHEMT LNAs' OIP3, DC current consumption, and NF versus gate width

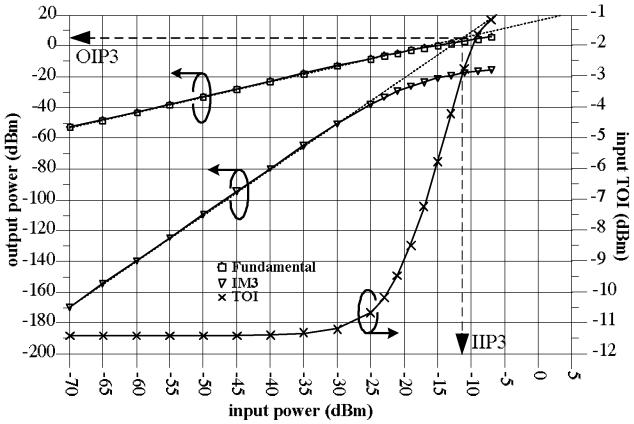

Figure 3. PHEMT LNA's simulated linearity and input-referred intercept point

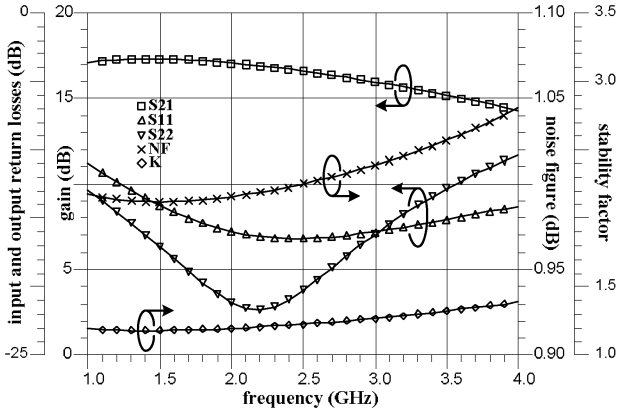

Figure 4. gain, input and output return losses, noise figure and stablity factor of PHEMT LNA

As can be seen in figure 4, the input and output is perfectly matched in a wide frequency band (over 4 GHz) to 50Ω impedance. The LNA has a gain equal to 16.6 dB at center frequency, and a gain over 14 dB and an NF of about 1 dB from RF up to 4 GHz. The PHEMT LNA draws a 28-mA current from a 3V DC supply.

B. Mixer

Half of a Gilbert cell is used as the mixer core for mixer topology. This topology has a single-ended RF input and differential IF outputs that are converted to single-ended operation with a balun circuit (external L_{balun1} and L_{balun2}, and integrated C_{balun}). Because of low IF signal frequency, the inductors required could not be realized on-chip.

In order to maintain a good linearity of the receiver path, the mixer must show very low intermodulation distortion. Additionally, a low noise figure is desired. Most active mixers suffer from a high noise figure and to maintain a good linearity, a relatively high current is required. A moderate LO power of -5 dBm is sufficient to achieve a conversion gain of +2.4 dB and the dual side band (DSB) noise figure of 6.7 dB. However the gain of the LNA is high enough so that the noise figure of the Rx mixer would not to be a critical parameter.

The single balanced mixer has an input 1-dB gain compression point (P_{1dB}) at -10 dBm and an input-referred third-order intercept point (TOI) of +2 dBm (figure 5).

In figure 6, output power gain as a function of the IF frequency is shown with the RF frequency fixed at 2400 MHz and LO frequency swept by VCO. The maximum conversion gain of 2.4 dB is measured at 340-MHz IF. The input and output return losses are shown in figure 6 in terms of dB. The RF and IF port return losses are better than -24dB and -8 dB, respectively, in the desired band.

The increase of the bias voltage of Q_1's gate results in the increase of gain, the increase of minimum NF and also the decrease of linearity in this single-balanced mixer topology. The input, output and LO ports impedances are all very close to 50Ω.

The potential advantage of using a micromixer is its low power consumption, where the mixer consumes only 5.3 mA at 3V DC supply. This active mixer results a very low LO-to-RF coupling equal to 57-dB port-to-port isolation that avoids from interfering. It also showed an LO-to-IF port isolation of about 36 dB.

The receiver mixer has inductive degeneration (L_S) to ground provided by on-chip 4.8-nH spiral inductor. The degeneration helps to achieve the linearity and matching requirements while maintaining lower noise figures in the receiver.

III. Simulation Results

The whole receiver RF front-end is developed in a 0.2-μm GaAs PHEMT MMIC technology for a center frequency of 2.4 GHz. The nominal power consumption is about 84 mW for the LNA and 16 mW for the mixer. The simulated S_{11} of the receiver chain demonstrates proper matching conditions as well as the power gain for the receiver chain (table 1).

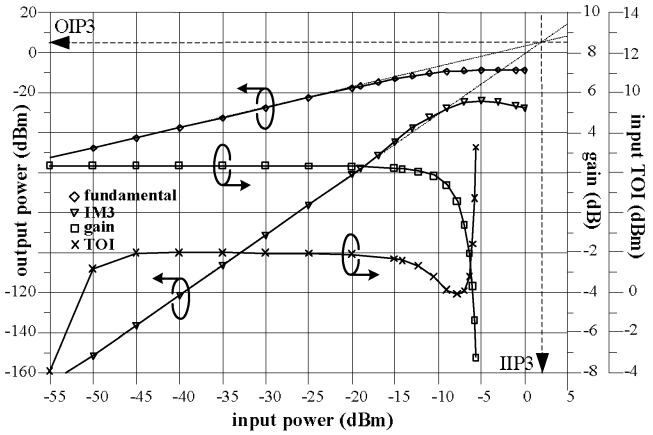

Figure 5. linearity, gain and TOI of mixer

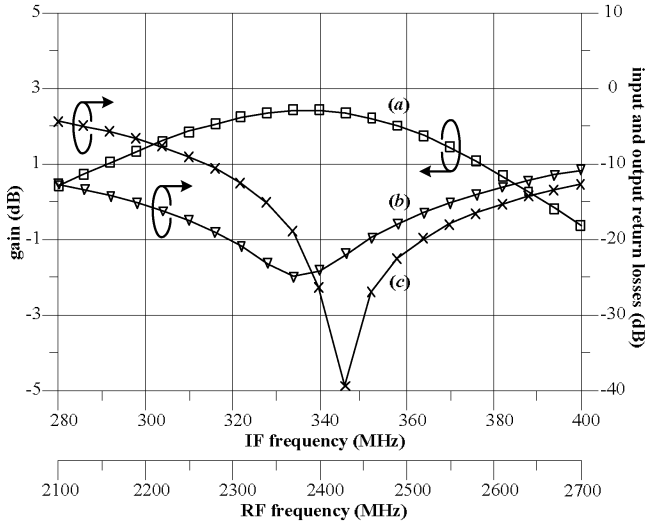

Figure 6. PHEMT mixer's (*a*) gain versus IF frequency, while LO frequency is sweeping and RF frequency is maintained constant (*b*) output return losses versus IF frequency, while LO frequency is sweeping and RF frequency is maintained constant (*c*) input return losses versus RF frequency, while RF frequency is sweeping and LO frequency is maintained constant

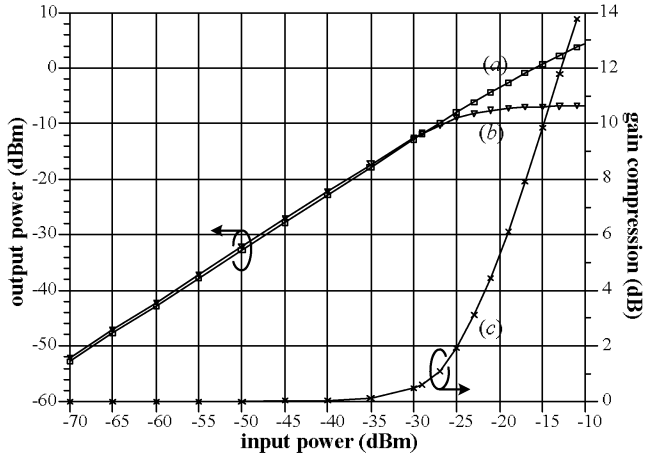

Figure 7. (*a*) LNA linearity (*b*) mixer output: front-end linearity (*c*) front-end input-referred gain compression

Figure 7 shows linearity budget analysis of receiver blocks with the overall gain compression curve which has been evaluated through RF system simulations. The P_{1dB} is at -27 dBm for input power. The system showed an IIP3 equal to -18 dBm and an NF equal to 1.8 dB with a 17.9-dB gain at 2400-MHz RF frequency and 2060-MHz LO frequency.

IV. CONCLUSION

The 2.4GHz MMIC receiver RF front-end building blocks reported on this paper was realized within a GaAs PHEMT Technology. The simulations result a good performance of the front-end system such as very low overall noise figure as well as an acceptable power consumption of better than 100 mW which meets the requirements for the portable wireless applications. The summarized results are given in table 1 with the results from a front-end with the same blocks topology in an 0.35-μm SiGe BiCMOS process, presented in [6], as a case of comparison. As can be seen from the table 1, the PHEMT LNA and mixer shows better noise figure and wider matching band than those of HBT ones. The improvements can be seen with comparing the specifications.

As a suggestion for improving the receiver performance against the strong input signals which can cause distortions, the switching-gain structure for the LNA given in [7] may be a proper choice. It helps to perform RF attenuation depending on received signal strength. As can be seen in [7], using an active matching at input can give an advantage of preserving input impedance near to 50Ω even in low-gain mode, but with the penalty of an increase in LNA noise figure which causes an increase in the overall receiver noise figure according to the Frii's equation.

In addition, the external BPF can be integrated in the front-end chip by substituting that with an active MMIC RF filter as desired.

TABLE I. GAAS P-HEMT FRONT-END COMPONENTS PERFORMANCE SUMMARY VERSUS SIGE HBT FROUNT-END COMPONENTS IN [7]

block	Parameters	GaAs PHEMT tech.	SiGe BiCMOS tech,	units
LNA	gain	16.6	15.5	dB
	NF	1.0	2.3	dB
	IIP3	-11.4	+2.4	dBm
	S11	<-16.5	<-20	dB
	S22	<-20.6	<-20	dB
	S12	-22.5	-	dB
	Power cons.	84	28	mW
mixer	gain	2.4	6.8	dB
	NF (DSB)	6.7	10.7	dB
	IIP3	2	-0.1	dBm
	S11@2400MHz	-24	-28	dB
	S22 @340MHz	-24	-40	dB
	S33 @2060MHz	-30	-	dB
	Power cons.	16	2.3	mW
system	gain	17.9	20.3	dB
	NF	1.8	4.4	dB
	IIP3	-18	-15.4	dBm
	S11	<-16	<-20	dB
	S22	<-24	<-35	dB
	Comp. point	-27	-27.5	dBm
	Power cons.	100	30	mW

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