DSP Control of UPS Inverter with Over-current Limit using Droop Method

Myung S. Moon and Robert W. Johnson
Powerware Corporation, Technology Center,
3201 Spring Forest Rd., Raleigh, North Carolina, 27616
Tel:919-871-1941, FAX:919-878-2385

Abstract-In this paper, a switched mode PWM inverter control using a fixed-point digital signal processor (DSP) for an uninterruptable power supply is presented. Issues related with a real-time digital control design of an inverter system and a pulse width modulation (PWM) with a fixed point DSP are discussed. And it is shown that the programmability of a DSP facilitates implementing the over-current limit control with a droop method. The simulation and experimental results are presented to verify.

I. INTRODUCTION

For a typical uninterruptable power supply (UPS) system, a switched mode inverter system with pulse width modulation (PWM) based on batteries is utilized to generate a pure sinusoidal AC output voltage for a certain load when the utility power is not present. In designing such an inverter, whether it is for a line-interactive mode or an online mode UPS system, minimizing the inverter filter size and weight becomes an important issue without compromising the system performance. However when we try to make a filter size smaller, which would reduce system size and weight as well as cost, the filter resonant frequency increases and the closed loop system bandwidth is widened. In fact, this prohibits the use of digital control with typical microprocessors because the sampling interval for the analog to digital (A/D) conversion and real time compensation introduces so excessive phase lag that it destabilizes a feedback control loop[1]. It is known that most of the power converter control with a microprocessor have a comparably large output power filter to minimize the effect of phase lag due to A/D conversion[1][2][3]. Owing to the advent of a fast digital signal processor, which is especially targeted to a switched mode PWM inverter application, a higher closed loop system bandwidth can be allowed with a digital compensator design and it is even possible to include the pulse width modulator inside a DSP chip with A/D converters, etc.[4]. In addition, since programmability of the DSP chip offers flexibility in designing a control loop, it is much easier to incorporate an advanced control algorithm, which can hardly be implemented with its analog counterpart.

In this paper, a switched mode PWM inverter control for a UPS application is presented. An approach for the digital real time control for inverter output voltage is as follows; an analog control design for the inverter voltage mode control is determined first as a reference design. Then its digital implementation is found. If necessary, the analog reference design is revised to resolve issues related with a fixed-point processor control design as well as the sample and hold delay. The over-current limit control is designed later exploiting the ease of programmability of DSP. Regarding the over-current limit control, when an over-load condition occurs, drooping the voltage reference can be easily implemented by utilizing a multiplier in a DSP, which is also important in digital filtering as well as interpolation algorithm associated with a lookup table.

In the next section, a full bridge inverter system based on batteries is presented briefly and its model is identified for a feedback control design. The voltage mode feedback control method of the inverter is described, and the control block diagram and a control model is found. In the third section, issues related with a digital control design of switched mode inverter system with the fixed-point DSP are discussed and resolved. Additionally the current limit strategy using a droop method is developed in conjunction with the voltage mode feedback control in the fourth section. Simulations and experimental results are provided for its verification.

II. UPS INVERTER SYSTEM DESCRIPTION AND VOLTAGE MODE CONTROL

In Fig. 1, a single phase PWM inverter is shown, where a battery delivers a necessary power to a critical load when a

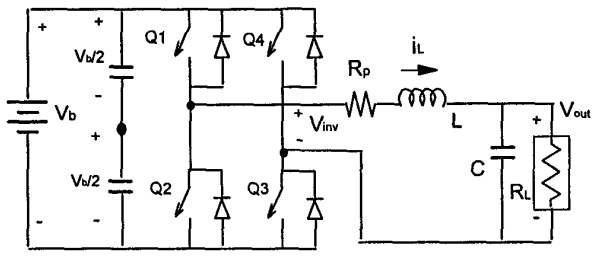

Fig. 1. Single phase PWM inverter for a UPS system

0-7803-5421-4/99/$10.00 © 1999 IEEE

utility line is failed. The full bridge inverter switch pairs, (Q1, Q3) and (Q2, Q4), are turned on/off simultaneously. As a result the inverter voltage V_{inv}, can be either positive rail voltage $+V_b/2$ or negative rail voltage $-V_b/2$. By the use of a PWM method, the inverter switch pairs can be controlled so that the inverter voltage may contain a fundamental line frequency voltage on top of carrier frequency ripple voltage. Through the low-pass filter, only the fundamental frequency voltage can be extracted to provide a near-pure sinusoidal voltage to a load. Since the low-pass power filter is a lightly damped second order system, the feedback control is required to provide stable and regulated inverter output voltage regardless of loads. The low pass filter transfer function from V_{inv} to V_{out} can easily be derived as

$$G(s) = \frac{1}{LCs^2 + (R_pC + L/R_L)s + 1 + (R_p/R_L)} \qquad (1)$$

Fig. 2 shows a PWM, where the inverter control command is compared with a triangular carrier signal to drive inverter switches and to shape the inverter output voltage. From Fig. 2, it is known that the PWM carrier signal height, h, would eventually represent the peak-to-peak value of the inverter output voltage and thus an inverter gain, K, in an average sense can be found as

$$K = \frac{V_b}{h} \qquad (2)$$

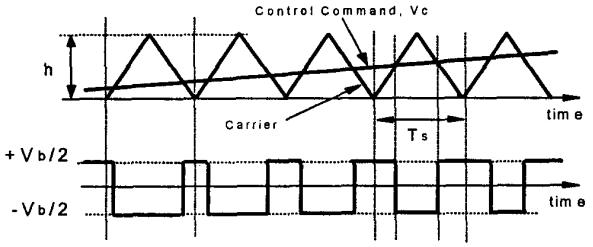

Fig. 2. PWM switching signal generation

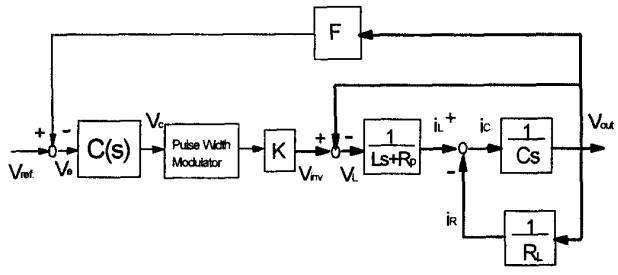

Fig. 3. Block diagram for voltage mode control

Based on the observation, a voltage mode feedback control block diagram is drawn, which is illustrated in Fig. 3. From the figure, the inverter voltage is sensed through a sensor with gain, F, compared to a sinusoidal reference, V_{ref}, to generate an error signal. It is known that from the figure, the filter transfer function V_{inv} to V_{out} was decomposed in order to extract the filter inductor current information. Also note that both the voltage reference signal amplitude and the sensor gain should be scaled such that the PWM carrier signal covers enough dynamic range of the control command. This is more important when we implement a fixed-point DSP control as will be discussed later. By considering the error transfer function V_{ref} to V_e,

$$\frac{V_e}{V_{ref}} = \frac{1}{1 + C(s)\,F\,K\,G(s)} \qquad (3)$$

the analog error signal compensator $C(s)$ can be designed by a loop gain analysis in the frequency domain so that a fast, stable, near pure sinusoidal inverter output voltage is obtained. This requirement can be achieved by keeping the crossover frequency higher, the phase margin higher, the feedback loop gain at line frequency higher, and the feedback loop gain at switching frequency lower. However since this analog control design will be a reference for a digital control design, this design approach may need to be modified to accommodate the digital control implementation. The analog feedback loop gain will be provided later to compare with its digital counter part.

III. DIGITAL CONTROL OF SWITCH MODE INVERTER

It is observed that the switched mode PWM power conversion scheme with the power lowpass filter has all the fundamental elements of digital system, both an analog to digital converter (ADC), which corresponds to a pulse width modulator, a digital to analog converter (DAC), which corresponds to switching devices and a power lowpass filter. But because of the nature of PWM in the switched mode

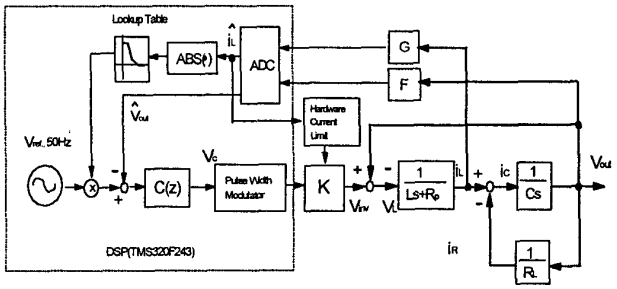

Fig. 4. Digital control block diagram

PWM power conversion scheme there exists no sample and hold delay as found in a conventional digital system. Thus we call it as analog PWM method.

In order to take advantage of DSP technology for a switched mode inverter application, the conventional digital control system can be incorporated for real time feedback control of a switch mode PWM inverter with various on-chip power electronic peripherals, such as an event manger for PWM, ADCs, etc. Particularly the PWM method with a DSP has a different characteristic from that of the analog PWM method due to the sample and hold delay introduced by a digital feedback control. In order to distinguish, it is called as digital PWM method. Based on the analog voltage mode control design as depicted in Fig. 3, the digital feedback control block diagram can be drawn and found in Fig. 4, where the over-current limit control portion to be discussed later is also shown. In the figure, the digital control components including a pulse width modulator are all embedded in a single DSP (TMS320 F243) chip as illustrated with a dotted box. This DSP is a 20MIPS 16bit fixed-point processor equipped with an event manager, 8 PWM channels, one multiplexed 10bit A/D converter, etc. In the dotted box of Fig. 4 the sensed discrete signals are differentiated by ($\wedge$) for its analog counter parts. The following factors are to be considered in designing and implementing a digital real-time feedback control with this type of application specific DSP.

A. *Sampling frequency and A/D converter*

Depending on the CPU speed of DSP core, the number of instructions per sampling period (NIPS) is limited as

$$NIPS = T_s \times CPU\ speed, \qquad (4)$$

where T_s is a sampling time(=1/sampling frequency). Also because of A/D conversion time, the actual available NIPS is reduced so that

$$T_s > (A/D\ conversion\ time + \frac{actual\ available\ NIPS}{CPU speed}) \qquad (5)$$

This means that within a given sampling period any sensed feedback signal needs to be converged to a certain stable discrete number in a A/D converter. And based on the A/D sampled number the control command calculation and the PWM gate drive signal generation must be completed before the next cycle. It is noted that generally when a cost constraint is a bigger concern, the DSP CPU speed and A/D conversion time would be limited so that the sampling time has to be compromised with the computational burden in a DSP for real time control. In addition it is known that the sampling frequency introduces a sample and hold delay as a form of phase lag as follows[8];

$$Phase\ lag = T_s \times f_c \times 360°, \qquad (6)$$

where f_c is the crossover frequency of a feedback loop gain. Since this phase lag is purely from digital control and takes up the phase margin of the given analog system, it is important that the analog prototype control design has sufficient phase margin. A cheaper and faster DSP in conjunction with fast ADC will allow a wider control bandwidth and a better control performance. The bit resolution of A/D converter is also important to minimize quantization effect. A 10bit A/D conversion for TMS320F243 will result in 0.1% error in the output, which may be significant especially in a high voltage application. With regard to selecting the switching frequency, both the filtering requirement and the power converter efficiency need to be considered to keep the switching frequency as high as possible. When a single DSP is utilized for both control and PWM, it may be possible to have a switching frequency different from the sampling frequency. However since the digital control design approach in this work is based on an analog control design prototype, we use the same frequency for both sampling and PWM switching for ease of implementation. In fact it provides a benefit in that neither a notch filter nor a lowpass is needed to sense nearly ripple-free current information as described in the next subsection.

B. *Digital pulse width modulation in a DSP*

The digital PWM method is explained by looking at Fig. 5. The triangular carrier signal in the analog PWM method shown in Fig. 2 is replaced by a digital timer with up/down count in a DSP (TMS320 F243) as seen in Fig. 5(a), in which both the analog control command and the digital control command are depicted for comparison. Note that although the digital control command may be a little different because the control command is determined dynamically based on a feedback information every sampling cycle, in order to explain the digital PWM method easier, a quantized version of the analog control command is considered as a digital

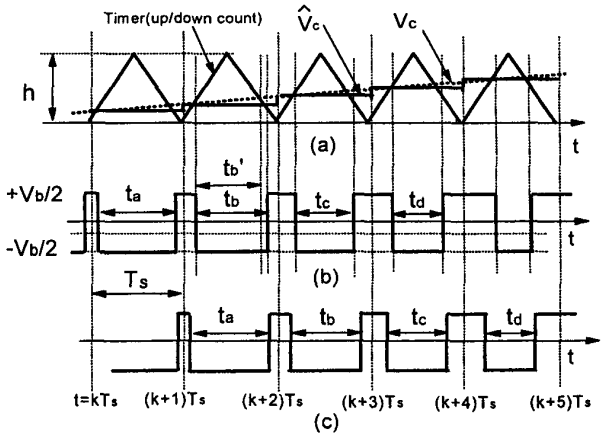

Fig. 5. Digital PWM method

PWM control command. From Fig. 5, for example suppose that a feedback signal is taken at $t=kT_s$, where k is a time sequence, the digital command control is calculated by $(k+1)T_s$ and the corresponding PWM takes effect after $(k+1)T_s$. Therefore there exists always time delay of T_s that would result in phase delay discussed earlier. This is shown from Fig. 5 (b) and (c). Also it is observed that the negative pulse width between $(k+1)T_s$ and $(k+2)T_s$ should have been t_b' if it were based on analog PWM. But because of the qunatization effect in digital PWM the pulse width is found to be t_b. In a worst case with this type of modulation this delay due to quantization error can be as much as $T_s/2$ which would increase phase lag. Therefore an analog prototype compensator needs to have enough phase margin so that its transformed digital compensator guarantees a stable feedback control. Also note that as can be speculated from Fig. 5, even though the inductor current would contain large ripple current, because an A/D converter synchronized with the switching frequency senses the inductor current nearly in the middle of the current ripple, an average inductor current is sensed so that neither no additional ripple filter is required. This implies that an A/D converter functions as an inherent notch filter.

C. *Scaling and Sensor Gain*

When a fixed-point DSP is used for a digital real time control, the signal scaling becomes more important. In order to support a dynamic range of signals and control parameters as wide as possible, at first the sensor gain needs to be determined so that the feedback signal covers voltage range of the A/D converter sufficiently. Then a digital filter structure must be chosen properly to have filter parameters well within the fixed-point number range and to prevent overflow error in the middle of filtering algorithm. Also the fractional number representation with Q15 format as well as overflow mode is utilized for digital compensation algorithm implementation to prevent overflow[7]. The TMS320F243 has a built-in overflow mode. By enabling the overflow mode, a calculated result can never be bigger than the most positive number or smaller than the negative number but is saturated. This type of saturation nonlinearity can be tolerated as long as the given linear system is stable and its transfer function is strictly proper[6].

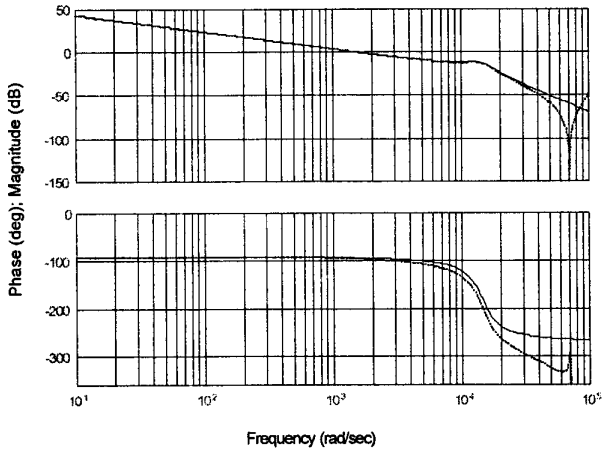

Fig.6. Bode plots of feedback loop gain

D. *Compensator transformation and closed loop gain*

Based on the analog control design, the digital filter,

$$C(z) = Z(C(s))_{T_s=45\mu sec} = 1100\frac{z+1}{z-1} \qquad (6)$$

where $Z(\bullet)_{Ts}$ represents Z-transformation, can be easily found using MATLAB, considering a given sampling time T_s=45μsec. Various transformation methods can be applied and we use the bilinear transformation method to duplicate the analog control design as closely as possible. Based on the digital filter transfer function in (6), the Bode plot of the feedback loop gain is provided with its analog counter part in Fig. 6, where the analog case is shown with a solid line and the digital case with a dotted line. For the Bode plot of the feedback loop, the filter parameters were given as L=500uH, C=10μF, Rp=2.5Ω for 380V rail voltages and 230Vrms output with a 700W load. As can be seen, the crossover frequency is 243 Hz and the phase margin is 85°, which minimizes the effect of sample and hold as well as the over-current limit control shown next.

IV. OVER-CURRENT LIMIT CONTROL

Occasionally when excessive loads are attached to the UPS, the UPS inverter will deliver excessive current because the feedback controller tries to regulate the nominal output voltage if the feedback control is robust enough. This high current is adverse to the switching devices in the inverter.

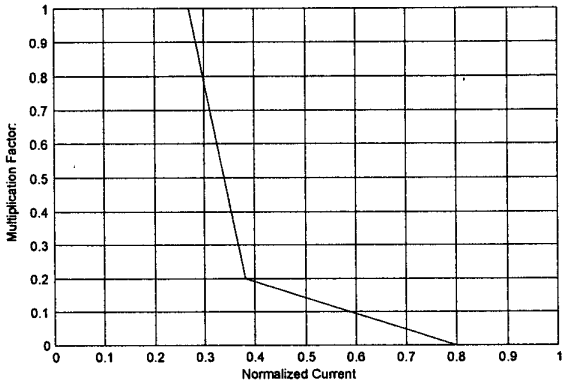

Fig. 7. Lookup table for over-current control

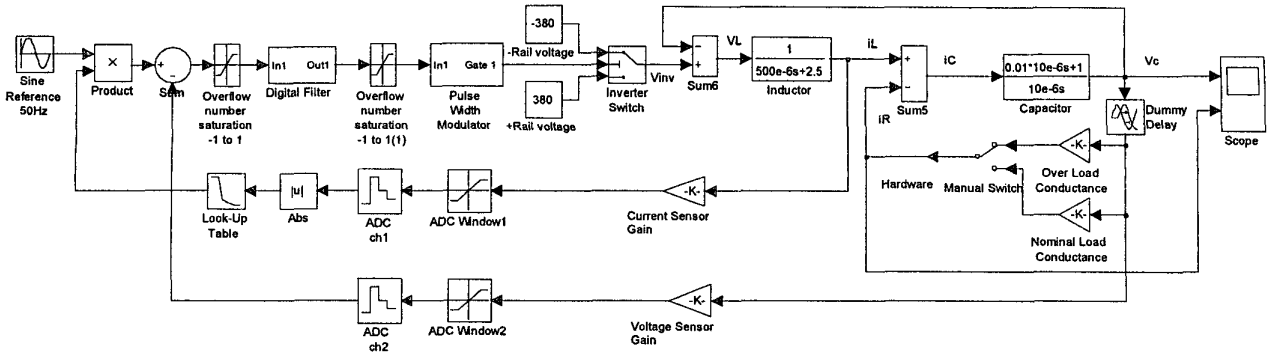

Fig. 8. MATLAB/SIMULINK simulation model

In this case when the UPS load causes excessive current, if the inverter output voltage is forced to have smaller amplitude, it is possible to limit the power delivered to a load. In order to implement this method, an inductor current needs to be sensed through a current transformer. With the sensed inductor current information the amplitude of the sine reference is determined by a lookup table. From the table, when the fundamental component of the inductor current is within a given specified range, multiplying a unity number makes no amplitude adjustment. However as the fundamental component of the inductor current is increased beyond the given range, a smaller number than one is found from a lookup table and multiplied to the voltage sine reference to reduce the amplitude of the sinusoidal reference, which would eventually reduce the inverter output voltage. The normalized current is used for fixed-point DSP calculation with fractional number format and calculated as follows,

$$i_{norm} = \sqrt{2}\, i_{rms} / G, \qquad (7)$$

where i_{rms} is the RMS current for nominal power and G is the current sensor gain. And a lookup table is established as seen in Fig. 7. Then an interpolation algorithm is required and can easily implemented with a DSP utilizing a multiplier. It is noted that an instantaneous current limit circuit may be required in order to protect inverter switches from the a peak current during a transient. Also it is important that in the feedback control design the voltage loop does not interfere with the voltage reference change when a over-load condition occurs.

V. SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the control technique and its DSP implementation, a simulation is conducted with a MATLAB/SIMULINK model as shown in Fig. 8. Note that we can incorporate the digital and nonlinear elements in the simulation by using MATLAB/SIMULINK. Its results are provided in Fig. 9. Fig. 9 (a) and (b) show the inverter

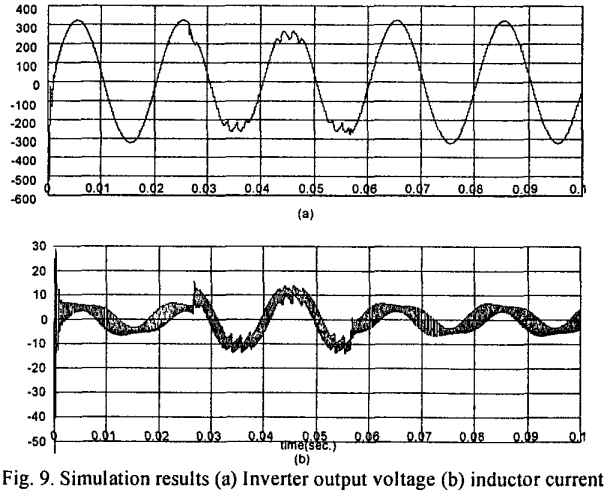

Fig. 9. Simulation results (a) Inverter output voltage (b) inductor current

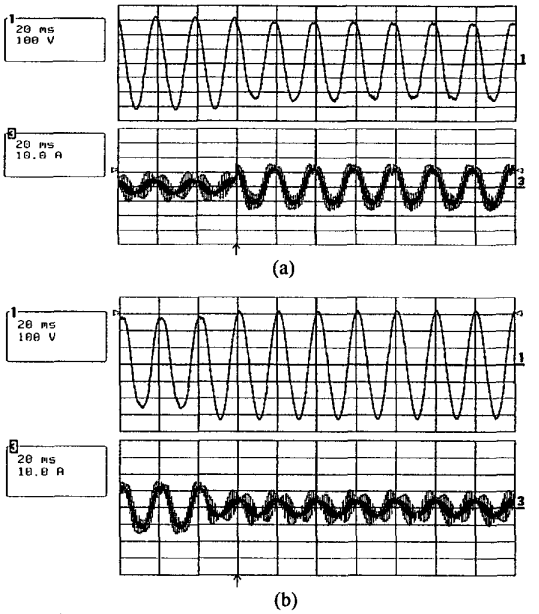

Fig. 10. Experimental results (a) nominal load to over-load (b) over-load to nominal load

output voltage and the inductor current response respectively. During the MATLAB/SIMULINK simulation, it is possible to change the load impedance value on the fly by using the manual switch in the figure. As can be seen in the simulation results, when the load is changed from 700W, a nominal load, to 2100W, the inverter output voltage drops from 330V fast while the inductor current is limited to 10A peak. As the load impedance is returned to its nominal value, the inverter output voltage is restored and the current level is dropped accordingly for a normal inverter operation. An experiment is set up as the simulation case and its results are provided in. Fig. 10(a) and (b). As shown, at the instant of load change from nominal load to three times of the nominal load, the output voltage droops so that the load current can be limited. As the inverter load is restored, the nominal inverter operation is returned fast with the help of DSP over-current limit control.

VI. Conclusion

In this paper, a DSP based digital feedback control for a switched mode PWM inverter was presented for UPS application. Issues related with a single fixed-point DSP chip solution including pulse width modulation and A/D converter for a digital control design of inverter system are discussed and resolved. As shown, not only the single chip solution simplifies the complete hardware implementation, but the programmability of the DSP chip facilitates both the voltage mode feedback control and the over-current limit control. The simulation and experimental results verify the effectiveness of the single-chip DSP control implementation.

Acknowledgment

The authors would like to thank to Joe Paulakonis, Powerware Corporation, Raleigh, North Carolina, for his assistance during the lab experiment.

References

[1] S. Buso, P. Mattavelli, L. Rosseto, and G. Spiazzi, "Simple Digital Control Improving Dynamic Performance of Power Factor Pregulators," *IEEE Trans. on Power Electronics*, Vol.13, No.5, Sept. 1998, pp.814-823.

[2] S. Jung, M. Chang, J. Jyang, H. Huang, L. Yeh, Y. Tzou, "Design and Implementation of an FPGA-Based Control IC for the Single-Phase PWM Inverter used in an UPS," *Power Electronics and Drive Systems*, 1997 International Conference on Volume: 1 , Page(s): 344 -349 vol.1.

[3] N. Abdel_Rahim and J. Quaicoe, "Analysis and Design of a Multiple Feedback Loop Control Strategy for Single-Phase Voltage-Source UPS Inverters," *IEEE Trans. on Power Electronics*, Vol.11, No.4, July, 1996, pp. 532-541.

[4] A. Mohammed, D. Figoli, and Z. Yu, "New Generation DSP Controllers Provide Cost Effective Motion Control Solutions," *PCIM*, February, 1998, pp.26-38.

[5] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, John Wiley & Sons, 1989.

[6] C. L. Phillips and H. T. Nagle, Digital Control System Analysis and Design, Prentice-Hall, 1990.

[7] H. K. Khalil, Nonlinear Systems, Macmilan Publishing, 1992.

[8] Texas Instrument Application Note, Implementing Digital Controllers, 1996.

[9] Texas Instrument Reference Set Volume 1 & 2 : TMS320C243 DSP Controllers, 1997.