

Deadbeat Controlled PWM Inverter with Parameter Estimation Using Only Voltage Sensor

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Abstract—A new control technique based on deadbeat control theory is proposed to obtain a nearly sinusoidal PWM inverter output voltage using only a voltage sensor. The closed-loop sampled-data feedback scheme inherently results in very fast response to load disturbance and nonlinear load, producing low total harmonic distortion. Parameter estimation of the plant provides a type of self-tuning of the proposed controller. A theoretical analysis and simulation and experimental results are presented for a single-phase PWM inverter controlled by an Intel 8086 microprocessor.

I. INTRODUCTION

THE ULTIMATE goal of the uninterruptible power supply (UPS) system is to supply constant amplitude sinusoidal voltage and constant frequency to a load without any interruption in case of a main power failure. The quality of the UPS output voltage is defined by the total harmonic distortion (THD). Historically, output transformer coupled stepped waveform techniques [1], [2], and programmed PWM techniques have been employed for minimization of either selected harmonics or THD [3]–[5]. However, these predecided control techniques have disadvantages: 1) the output voltage is very much distorted by nonlinear loads such as rectifier loads, and 2) the response time of the voltage regulation usually takes a few cycles for sudden application or removal of full load. Another approach is real-time waveform feedback control, such as the time-optimal response or instantaneous feedback control [6]–[8], which overcomes the aforementioned disadvantages and is quite simple to implement. However, this real-time control has other disadvantages: 1) high switching frequency is required for this scheme to achieve low THD, and 2) harmonic fre-

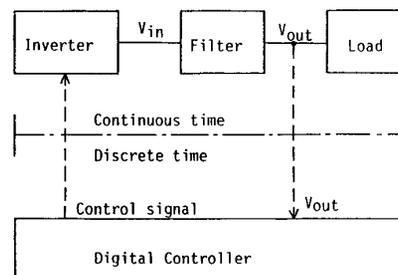


Fig. 1. Basic diagram of deadbeat controlled PWM inverter.

quencies are spread over a wide range around the average switching frequency.

The microprocessor deadbeat control approach in [9], which synthesizes the output waveform by digital feedback control, inherently results in very fast response to load disturbances and nonlinear loads and can be theoretically implemented at any reasonably high sampling frequency which is high relative to the output filter resonant frequency. A basic block diagram for a deadbeat controlled PWM inverter system is shown in Fig. 1, where the inverter- LC filter-resistive load is considered as the "plant" of a closed-loop digital feedback system with a sinusoidal reference. The microprocessor controls the inverter switches so that the output voltage is exactly equal to the sinusoidal reference at the sampling instants. Unlike the conventional system, this system does not use a programmed PWM pattern for the inverter output. Instead, the PWM pattern is determined at every sampling instant by the microprocessor based on output measurements and the reference. Thus a low THD sinusoidal output is obtained by using a feedback control technique rather than explicitly eliminating harmonics. The drawbacks of [9] are 1) at each sampling instant, detection of both output voltage and capacitor voltage current are required, 2) the feedback gains must be adjusted manually by trial and error because the theoretical plant parameters determined from the measured L , C , and R are not the true values, mainly due to nonlinear effects of the plant.

To solve these problems, this paper presents first the derivation of a new discrete-time state equation and then an output deadbeat control algorithm for the PWM inverter using only a voltage sensor. The controller uses voltage signals at the present and previous sampling in-

Manuscript received July 15, 1986; revised September 4, 1987. This paper was presented at the IEEE Power Electronics Specialists Conference, Vancouver, BC, Canada, June 1986.

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IEEE Log Number 8719065.

0885-8993/88/0400-0118\$01.00 © 1988 IEEE

stants, the pulsewidth signal from the previous sampling interval, and the reference signal for the next sampling interval, which may be called one sampling ahead preview control. Second, a parameter estimation method for the discrete-time state equation is proposed using the least square error algorithm, with the assumption of existence of a small amount of input white noise. Finally, simulation and experimental results are shown to verify the proposed scheme.

II. DEADBEAT CONTROL ALGORITHM WITH VOLTAGE SENSOR AND PARAMETER ESTIMATION

A. Deadbeat Control Law or One Sampling Ahead Preview Control

Fig. 2 shows the circuit diagram for the proposed scheme. The power circuit consisting of the inverter, LC filter, and resistive load R is modeled as a second-order system with state vector $[v_c \ \dot{v}_c]^t$, where v_c is the capacitor (output) voltage and \dot{v}_c is the derivative of v_c . Input v_{in} can take three values, $+E$, $-E$, or 0 . Equation (1) gives the state equation of the system:

$$\begin{bmatrix} \dot{v}_c \\ \ddot{v}_c \end{bmatrix} = A \begin{bmatrix} v_c \\ \dot{v}_c \end{bmatrix} + \vec{b} v_{in} \quad (1)$$

where

$$A \triangleq \begin{bmatrix} 0 & 1 \\ -\frac{1}{LC} & -\frac{1}{CR} \end{bmatrix} \quad \vec{b} \triangleq \begin{bmatrix} 0 \\ \frac{1}{LC} \end{bmatrix}. \quad (2)$$

As shown in Fig. 3, one period of the 60-Hz reference sine wave is divided into 30 equal intervals of duration T ($T = 555 \mu\text{s}$), the sampling interval of the system. As shown in Fig. 4, the power switches are turned on and off once during each interval T , such that the filter input v_{in} is a voltage pulse of magnitude E (or $-E$) and width ΔT centered in the interval T .

Using the assumption $T \ll 2\pi\sqrt{LC}$, the sampled data system can be derived from (1) [9]:

$$\begin{bmatrix} v_c(k+1) \\ \dot{v}_c(k+1) \end{bmatrix} = \begin{bmatrix} \phi_{11} & \phi_{12} \\ \phi_{21} & \phi_{22} \end{bmatrix} \begin{bmatrix} v_c(k) \\ \dot{v}_c(k) \end{bmatrix} + \begin{bmatrix} g_1 \\ g_2 \end{bmatrix} \Delta T(k) \quad (3)$$

where

ϕ_{ij} corresponding element of e^{AT}
 g_i corresponding element of $e^{AT/2} \vec{b} E$,
 $v_c(k)$, $\dot{v}_c(k)$, $\Delta T(k)$ their values at the sampling instant $t = kT$.

After Z-transforming (3), $v_c(z)$ becomes

$$v_c(z) = \frac{g_1 z + (g_2 \phi_{12} - g_1 \phi_{22})}{z^2 - (\phi_{11} + \phi_{22})z + \phi_{11} \phi_{22} - \phi_{21} \phi_{12}} \Delta T(z). \quad (4)$$

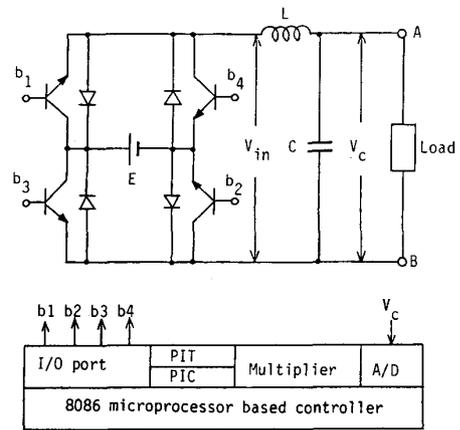


Fig. 2. Proposed PWM inverter system.

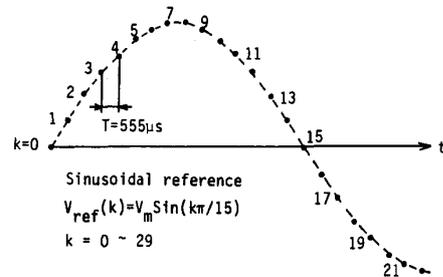


Fig. 3. Reference signal.

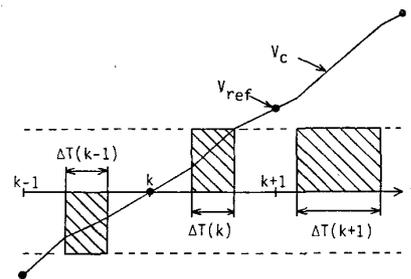


Fig. 4. Pulse pattern and output voltage.

Thus the following difference equation is obtained:

$$\begin{aligned} y(k) + a_1 y(k-1) + a_2 y(k-2) \\ = b_1 u(k-1) + b_2 u(k-2) \end{aligned} \quad (5)$$

where normalized variables and parameters are defined

$$\begin{aligned} y(k) &\triangleq v_c(k)/E \\ u(k) &\triangleq \Delta T(k)/T \\ a_1 &\triangleq -(\phi_{11} + \phi_{22}) \\ a_2 &\triangleq \phi_{11} \phi_{22} - \phi_{12} \phi_{21} \\ b_1 &\triangleq g_1 * T/E \\ b_2 &\triangleq (g_2 \phi_{12} - g_1 \phi_{22}) * T/E. \end{aligned}$$

By increasing k by one in (5), and replacing $y(k+1)$ with the reference signal $y_{\text{ref}}(k+1)$, the deadbeat control law is

$$u(k) = -\frac{b_2}{b_1}u(k-1) + \frac{a_1}{b_1}y(k) + \frac{a_2}{b_1}y(k-1) + \frac{1}{b_1}y_{\text{ref}}(k+1). \quad (6)$$

This equation implies that the required signals for determination of the pulsewidth $u(k)$ are the output voltage at the present and previous sampling instants ($y(k)$ and $y(k-1)$), the pulsewidth in the previous sampling interval ($u(k-1)$), and the reference signal at the next sampling instant ($y_{\text{ref}}(k+1)$). If the coefficients in (6) are exactly known, this deadbeat control law forces the output voltage to be exactly equal to the reference signal at the next sampling interval.

One problem with this control scheme is that coefficients a_1 , a_2 , b_1 , and b_2 are derived from the plant parameters R , L , C , and the sampling interval T with the assumption of linearization [9], so that the theoretically calculated values are slightly different from the true values even though R , L , C , and T are exactly known. Also, the nonlinear effects in the system, such as turn-on and turn-off delays of the switching devices, nonlinearity of the inductor, and the time delay in the software program, cause the coefficients to differ from theoretically predicted values. In addition to these effects, the load change apparently causes variation of these parameters. Thus parameter estimation in (5) is essential to make the proposed algorithm have a self-tuning ability for any plant parameter fluctuation.

B. Parameter Estimation

Equation (5) is a single-input-single-output difference equation, so that the least square error (LSE) algorithm is chosen to identify the parameters a_1 , a_2 , b_1 , and b_2 . The estimated parameters \hat{a}_1 , \hat{a}_2 , \hat{b}_1 , and \hat{b}_2 given by the off-line LSE algorithm are

$$\begin{bmatrix} -\hat{a}_1 \\ -\hat{a}_2 \\ \hat{b}_1 \\ \hat{b}_2 \end{bmatrix} = [\Omega^T \Omega]^{-1} \Omega^T \vec{y}_N \quad (7)$$

where

$$\Omega \triangleq \begin{bmatrix} y(1) & y(0) & u(1) & u(0) \\ y(2) & y(1) & u(2) & u(1) \\ \vdots & \vdots & \vdots & \vdots \\ y(N-1) & y(N-2) & u(N-1) & u(N-2) \end{bmatrix}$$

$$\vec{y}_N^T \triangleq [y(2) \ y(3) \ \cdots \ y(N)]$$

$$N \triangleq 30 \text{ (one cycle).}$$

This algorithm requires that the input $u(k)$ should satisfy the fourth-order persistently exciting condition [10], because the plant is second order. For example, if $u(k)$ is chosen as a single sinusoidal signal, which is the second persistently exciting signal, parameters cannot be identified. For this reason, the parameters cannot be estimated under the ideal deadbeat control. A very small amount of different frequency components or white noise (WN) should be added to the input u of the deadbeat controller so as to make the $u(k)$ greater than or equal to the fourth-order persistent excitation. The other approach is to supply only WN to the plant using the maximum period sequence (MPS) and identify the parameters.

III. SIMULATIONS AND EXPERIMENTAL RESULTS

A. Deadbeat Control

A digital computer simulation was carried out with the following circuit parameters:

$$\begin{aligned} \text{sampling interval } T &= 555 \mu\text{s} \\ \text{sampling frequency} &= 30 \times 60 \text{ Hz} = 1800 \text{ Hz} \\ \text{reference sine wave} &= 30 \text{ V peak at } 60 \text{ Hz} \\ \text{rated load current} &= 15 \text{ A} \\ E &= 40 \text{ V} \\ L &= 0.5 \text{ mH} \\ C &= 800 \mu\text{F} \\ R &= 2 \Omega. \end{aligned}$$

Theoretically calculated parameters in (5) are

$$\begin{aligned} a_1 &= -1.096 \\ a_2 &= 0.7066 \\ b_1 &= 0.3429 \\ b_2 &= 0.2882. \end{aligned}$$

Fig. 5 shows the digital computer simulated output waveform with 1.5-percent THD using the proposed deadbeat controller. Fig. 6 shows the experimental results with the same conditions as Fig. 5. The hardware arrangements of the experimental setup are similar to those in [9]. The parameters of (6) used in the experiments are experimentally estimated by the LSE algorithm, which is described in the following section. Fig. 6(a) is the inverter output waveform with 2.8-percent THD, and Fig. 6(b) is the harmonic spectrum of the output voltage in Fig. 6(a) measured by a Hewlett Packard 3561A Dynamic Signal Analyzer. The sampling frequency is 1800 Hz so that (1800 ± 60) -Hz harmonics are expected to be dominant. However, the third, fourth, and fifth harmonics are observed to be larger due to the nonlinearity of the inductor, unbalanced switching characteristics of the power transistors, and parasitic noise to the A/D converter. Table I illustrates the comparison of simulations and experiments.

To check the transient response of the proposed controller, a nonlinear load is connected—a triac with 100-percent resistive load. For example, if the firing angle is

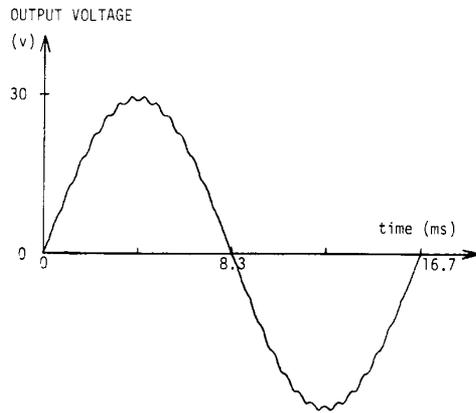
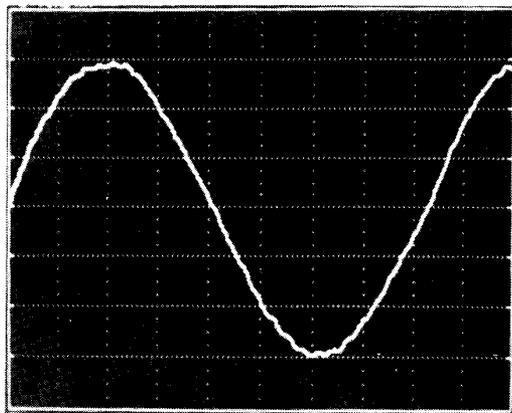
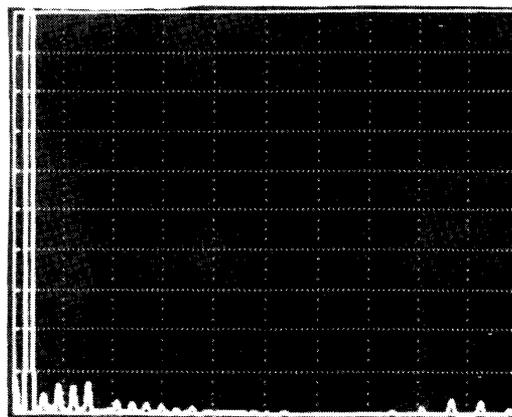


Fig. 5. Simulated output voltage waveform ($R = 2 \Omega$).



(a)



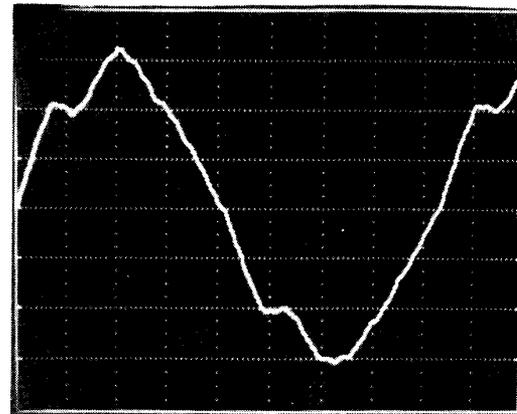
(b)

Fig. 6. Experiment with $R = 2 \Omega$. (a) Inverter output voltage waveform (vertical: 10 V/div; horizontal: 2 ms/div). (b) Harmonic spectrum of (a) (vertical: 2 percent/div; horizontal: 200 Hz/div).

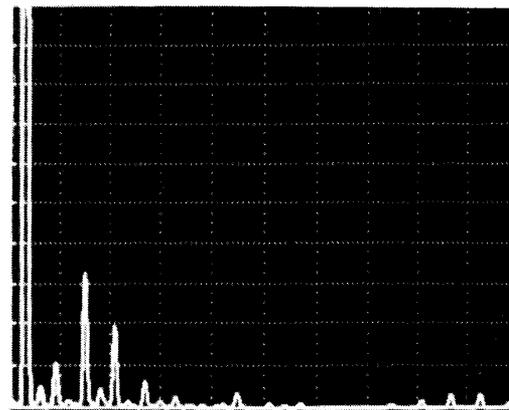
36° , no load is connected from 0 to 36° , and at the instant of 36° , a full resistive load is connected to the inverter until the end of the half-cycle. From that moment to 180° plus 36° again no load is connected, and from 180° plus 36° to 360° , full resistive load is applied.

TABLE I
COMPARISON OF SIMULATION AND EXPERIMENT RATED LOAD ($R = 2 \Omega$)
WITH $V_{ref} = 30 V_{peak}$

	Simulation	Experiment
Fundamental component (V_1)	29.4 V_{peak}	29.7 V_{peak}
Phase shift of V_1 (lag)	0.1°	$\approx 1^\circ$
THD	1.5%	2.8%
Waveform	Fig. 5	Fig. 6(a)



(a)



(b)

Fig. 7. Experiment with triac load (36°). (a) Inverter output voltage waveform (vertical: 10 V/div; horizontal: 2 ms/div). (b) Harmonic spectrum of (a) (vertical: 2 percent/div; horizontal: 200 Hz/div).

Fig. 7(a) and Fig. 8(a) show the output voltage with triac firing angles of 36° and 84° , respectively, and Fig. 7(b) and Fig. 8(b) are the resultant harmonic spectra. These results are summarized in Table II. These photos indicate that the transient response of the proposed dead-beat control for nonlinear load is only about three sampling intervals. Thus very quick response is achieved.

B. Parameter Estimation

Table III summarizes the simulation and experimental results for the parameter estimation in (5), using the LSE algorithm described in Section II-B. In the simulations a

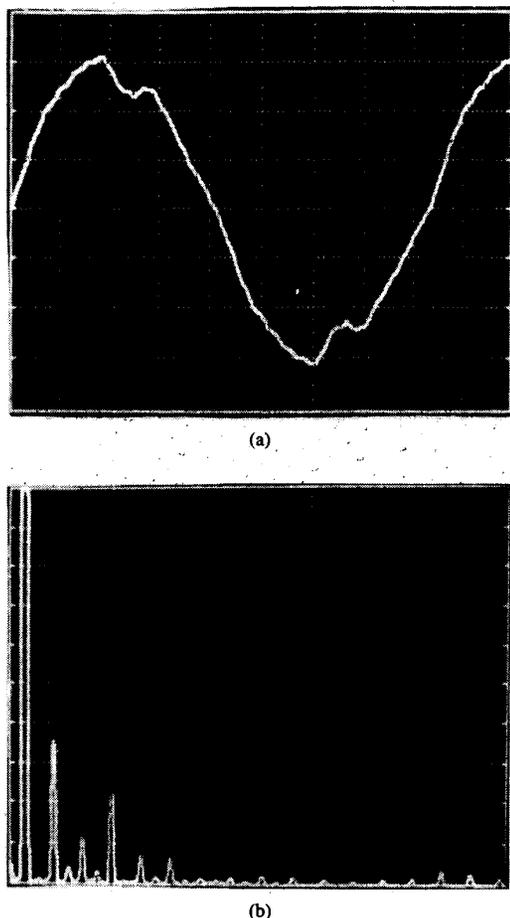


Fig. 8. Experiment with triac load (84°). (a) Inverter output voltage waveform (vertical: 10 V/div; horizontal: 2 ms/div). (b) Harmonic spectrum of (a) (vertical: 2 percent/div; horizontal: 200 Hz/div).

TABLE II
TRANSIENT RESPONSE TRIAC LOAD^a

Firing Angle (Degrees)	THD (Percent)	V_1 (Fund Peak) (V)	Transient
0	2.8	29.7	see Fig. 6(a)
36	8.0	28.6	see Fig. 7(a)
84	8.8	30.0	see Fig. 8(a)

^a $R = 2 \Omega$, $V_{ref} = 30$ V, controller gains are the same for all firing angles.

small amount of WN is superimposed on the input $u(k)$ after the deadbeat control law (6) is calculated. The parameters are well estimated with increased WN, but the THD is also increased.

From the viewpoint of the hardware implementation, the input $u(k)$ has inherent noise due to interrupt control of the system. The endings of the pulses $\Delta T(k)$ in Fig. 4 are triggered by a polling type of microprocessor interrupt. Thus the actual pulsewidth is not exactly the same as the desired pulsewidth; the error is on the order of two

TABLE III
PARAMETER IDENTIFICATION

Simulations—Deadbeat Control with White Noise Fundamental Output Voltage: 30 V Peak		
Ratio of WN Amplitude to Full Duty Ratio (Percent)	Estimated Parameter	THD (Percent)
0	N/A	1.5
2.5	$a_1 = -1.135$, $b_1 = 0.3164$ $a_2 = 0.7225$, $b_2 = 0.2810$	1.8
5	$a_1 = -1.120$, $b_1 = 0.3213$ $a_2 = 0.7174$, $b_2 = 0.2882$	2.6
Theoretical values	$a_1 = -1.096$, $b_1 = 0.3429$ $a_2 = 0.7066$, $b_2 = 0.2882$	1.5
Experiments—Only Pseudo White Noise Using Maximum Period Sequence		
Ratio of PWN Amplitude to Full Duty Ratio (Percent)	Estimated Parameter	
± 20	$a_1 = -0.9584$, $b_1 = 0.3523$ $a_2 = 0.5473$, $b_2 = 0.2946$	
± 10	$a_1 = -0.9147$, $b_1 = 0.3417$ $a_2 = 0.3467$, $b_2 = 0.1868$	

to three percent. However, the experiments with use of this noise resulted in large error in estimation of parameters due to other unexpected noise in the system, such as turn-on and turn-off delays of the switching devices. Thus a pseudo white noise (PWN) was artificially added to the input $u(k)$ using a maximum period sequence (MPS). With five-percent injection of PWN, parameters were still not well estimated, even though the inverter output voltage waveform was very much distorted. As a result of these investigations, only PWN was used as input $u(k)$ and then parameters were well estimated. The output voltage was close to zero with only the PWN input. Table III summarizes these experiments. A PWN of ten percent in the experiments means that ten-percent width of the positive or negative pulse in one sampling interval was generated, depending on "1" or "0" of the MPS output. The estimated parameters with 20 percent of PWN were used throughout all the experiments in this paper.

The experimentally estimated parameters by the LSE algorithm are different from theoretical values (see Table III). The feedback control gains in (6) with estimated parameters resulted in lower THD than with the theoretical parameters. Thus it is concluded that the experiential parameter estimation is a very useful approach to find the best feedback gains for deadbeat control at a given load condition. In the next section, the effect of detuning is discussed in case of load change.

C. Parameter Sensitivity of Deadbeat Controller

When the plant constants such as R , L , or C change, the parameters a_1 , a_2 , b_1 , and b_2 in (5) also change. Thus, if the deadbeat controller uses the feedback gains in (6)

which are adjusted to the previous plant constants, then the detuning problem occurs. This phenomenon is investigated from the viewpoint of theory, simulations, and experiments.

First, using (6), define a general digital control law as follows:

$$u(k) = -\frac{q_2}{q_1} u(k-1) + \frac{p_1}{q_1} y(k) + \frac{p_2}{q_1} y(k-1) + \frac{1}{q_1} y_{\text{ref}}(k+1) \quad (8)$$

where p_1 , p_2 , q_1 , and q_2 are feedback gains.

Next, taking the Z-transformation of (5) and (8) and eliminating $u(z)$ produces

$$y(z) = \frac{(b_1 z + b_2) z^2 y_{\text{ref}}(z)}{(z^2 + a_1 z + a_2)(q_1 z + q_2) - (p_1 z + p_2)(b_1 z + b_2)} \triangleq G(z) y_{\text{ref}}(z). \quad (9)$$

If p_1 , p_2 , q_1 , and q_2 are exactly equal to plant parameters a_1 , a_2 , b_1 , and b_2 , then (9) has two poles at zero, and one pole at the plant zero ($-b_2/b_1$). Thus (9) becomes

$$y(z) = y_{\text{ref}}(z). \quad (10)$$

This equation means that no time delay deadbeat response is obtained with a control law (8) using exactly tuned gains p_1 , p_2 , q_1 , and q_2 .

Now if the plant constants change after the controller gains in (8) are determined for the previous plant constants, then the poles in (9) shift a little from the desired values, which will cause detuning, and deadbeat response (10) is no longer obtained. The trajectories of poles and zeros in (9) are plotted in Fig. 9, when the load R changes its magnitude. Since the pole zero cancellation is not achieved, and also the poles move from the origin, the exact deadbeat response is not achieved. However, all poles are within a unit circle, so that stable operation is expected. Similarly, from numerical calculation it is confirmed that the system is stable as long as L is larger than 0.345 mH with $R = 2 \Omega$ and $C = 800 \mu\text{F}$, or C is larger than 650 μF with $R = 2 \Omega$ and $L = 0.5$ mH.

The frequency response of (9) also provides the information about the gain magnitude and phase shift at 60-Hz fundamental frequency. If the controller is tuned, the gain is unity and the phase shift is zero degrees, as is obtained for (10). By changing the load resistance R , and maintaining the other parameters constant, the effect of the detuning in the frequency domain is obtained using the Bode plot. The gain and phase at 60 Hz are plotted in Fig. 10, by changing R . This figure shows that the gain is almost unity and the phase becomes leading as the resistance increases. Thus, from Figs. 9 and 10, it is expected that the detuning due to load change may affect the deadbeat response, but stable operation may still be achieved.

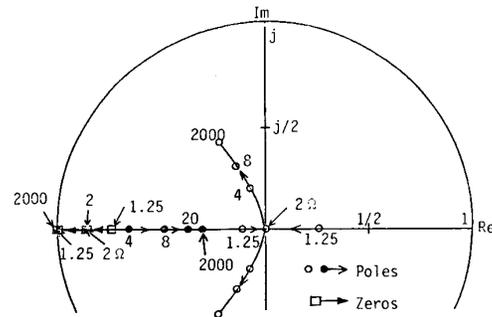


Fig. 9. Trajectories of poles and zero of (9) with R change in z domain.

Simulation and experimental results are summarized in Table IV with various linear load conditions. The pure resistive load was changed from the rated value to almost no load. The THD did not change so much both in simulations and experiments. Next, $R-L$ and $R-C$ loads were selected, and again almost similar THD was obtained both in simulations and experiments. For all of these experiments, the system was very stable.

D. Discussion

In general, a deadbeat controller is believed to be very sensitive to parameter variations. However, the proposed controller synthesizes the sinusoidal waveform with almost constant THD under various load conditions—rated resistive load, open load, and $R-L$ and $R-C$ loads. The authors believe this insensitivity is due to the following:

1) The LC filter is large enough to minimize the effect of impedance change of the load.

2) The inverter pulse pattern itself is a nonlinear operation, and this nonlinearity inherently sustains a stable oscillation of the output voltage within each sampling interval (see Fig. 4). This oscillation may reduce the effect of load variations. In other words, it is impossible to achieve a state-deadbeat response, i.e., control of both v_c and i_c , even though it appears to be possible in the linearized state equation (3).

For this reason, an on-line parameter estimation may not be necessary unless a very precise output waveform control is required.

IV. CONCLUSION

A deadbeat controller, or more exactly, an output feedback one sampling ahead preview controller, is proposed

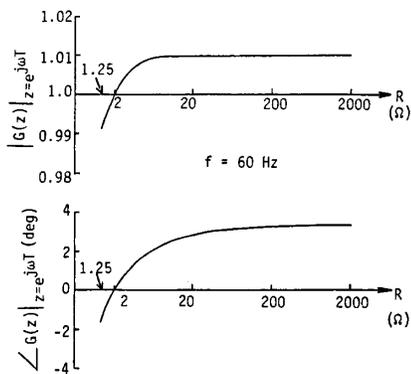


Fig. 10. Magnitude and phase of (9).

TABLE IV
PARAMETER SENSITIVITY (LINEAR LOAD)

Simulations— $V_{ref} = 30$ V, Controller Gains are the Same for the Following Simulations			
Different Loads	THD (Percent)	V_1 (Fund Peak) (V)	Phase Shift (Degrees)
100-percent load ($R = 2 \Omega$)	1.5	29.4	0.1 (lag)
0.1-percent load ($R = 2 \text{ k}\Omega$)	1.4	29.7	3.1 (lead)
RC load ($1.6 - j 1.2 \Omega$)	0.7	30.7	0.2 (lead)
RL load ($1.6 + j 1.2 \Omega$)	1.5	28.6	0.9 (lead)
Experiments— $V_{ref} = 27$ V, Controller Gains are the Same for the Following Experiments			
Different Loads	THD (Percent)	V_1 (Fund Peak) (V)	
100-percent load ($R = 2 \Omega$)	2.9	26.9	
1-percent load ($R = 200 \Omega$)	2.4	29.3	
No load ($R = \infty \Omega$)	2.4	29.3	
RC load ($1.96 - j 0.29 \Omega$)	3.1	27.2	
RL load ($1.4 + j 0.75 \Omega$)	3.1	25.6	

to produce a low THD sinusoidal voltage for a single-phase PWM inverter. The performance was theoretically analyzed, simulated by digital computers, and finally demonstrated using an 8086-based experimental setup. Next, a parameter identification algorithm was implemented to select the best gains, and these values were used in the experiments. The advantages of the proposed scheme are:

- 1) low THD,
- 2) very fast transient response,
- 3) only voltage sensing is required,
- 4) stable operation for various load conditions, and
- 5) applicability to three-phase systems.

The applications of the proposed scheme are UPS systems and ac adjustable speed drive systems with GTO, SCR, and power transistor switching devices, where precise output voltage regulation and fast transient response are required. The proposed controller originates a new class of microprocessor applications to power conversion techniques.

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Design-Oriented Analysis of Boost Zero-Voltage-Switching Resonant DC/DC Converter

MARIAN K. KAZIMIERCZUK

Abstract—The analysis and design procedures are presented for a boost high-efficiency high-frequency zero-voltage-switching resonant dc/dc power converter. The equations describing converter operation are derived. The basic performance parameters of the circuit are analyzed as functions of the normalized load resistance and switching frequency. Those equations are then used to determine conditions for lossless converter operation and design equations which yield the required component values.

I. INTRODUCTION

CONVENTIONAL PWM dc/dc power converters have recently been modified by adding a resonant circuit [1]–[9]. This modification of the converter circuits allows the voltage waveform to be shaped across the switch in such a way that the transistor turns on at zero voltage, similarly as in Class E tuned power amplifiers and Class E dc/dc converters. In addition, the transistor output capacitance, the leakage transformer inductance, and most of the other parasitic components are absorbed into the converter topologies. Therefore, the turn-on switching loss is reduced to zero, yielding high efficiency (up to 90 percent) at switching frequencies higher by a factor of about 100 compared to the PWM converters. Thus the zero-voltage-switching technique offers a new means of highly efficient dc-to-dc energy conversion at higher frequencies and a higher power-to-volume coefficient which is greatly desirable in many practical applications. Fig. 1 shows a block diagram of zero-voltage-switching [1]–[9] and zero-current-switching converters [10]–[12]. The dc output voltage V_o in all these converters is controlled by varying the switching frequency f . Therefore, they are called frequency modulated (FM) converters. This paper expands upon the previous publications [1]–[9] by providing an analytical basis for operation of the boost converter, along with design equations.

The basic circuit of the boost zero-voltage-switching resonant dc/dc converter is shown in Fig. 2(a). It consists of a switch S , a rectifier diode $D2$, a resonant circuit LC , a large inductor L_f , and a large capacitor C_f . R_L is a load to which the dc power is to be delivered. The switch S is composed of a switching power transistor (a FET or a BJT) and an antiparallel diode $D1$ as shown in Fig. 3(a),

Manuscript received March 16, 1987; revised September 14, 1987. This work was supported by Wright State University under Grant 241-262.

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IEEE Log Number 8719066.

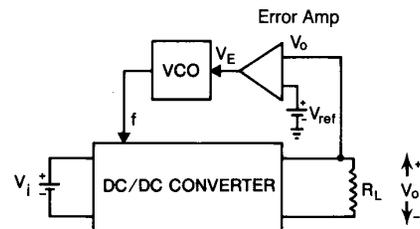


Fig. 1. Block diagram of zero-voltage-switching and zero-current-switching FM resonant dc/dc power converters.

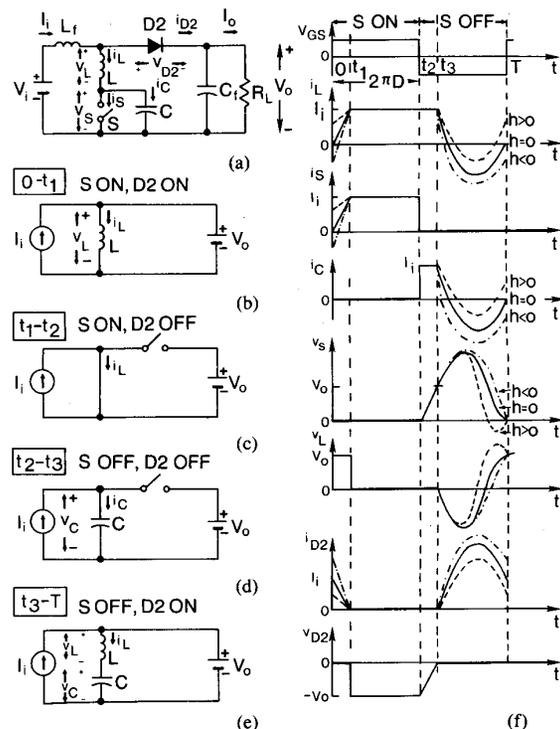


Fig. 2. Boost zero-voltage-switching resonant dc/dc converter. (a) Circuit. (b)–(e) Models. (f) Steady-state waveforms.

or a transistor and a series diode $D1$ as shown in Fig. 3(b). In the first case, S is a bidirectional switch for current, whereas in the other case, S is a bidirectional switch for voltage [2]–[4]. Circuit operation is determined by states of S and $D2$ and the transient response of the resonant circuit LC . Two switches, S and $D2$, give four combinations of the states. Therefore, four time intervals of