Impact of High Resolution Lithography on IC Mask Design

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Introduction

Not only are shrinking device dimensions placing increasing technology challenges on existing lithography processes, but they are also forcing changes in the layout and masking approaches that support them. The need to extend traditional optical lithography to 180nm using resolution enhancing technologies such as optical proximity correction (OPC) or phase shift masks (PSM) generally requires the use of pattern modifications that are not part of the original design layout. Furthermore, implementation of new post-optical lithography techniques may require significant changes in reticle layout formats in addition to fundamental material and process changes. For example, new formats are required for masked E-beam (SCALPEL) and ion projection lithography reticles, while very high resolution OPC appears to be necessary to extend 1X X-ray lithography below 100nm. However, unlike the case with OPC and PSM extensions for optical lithography, design tools to support new post-optical patterning formats have not yet been developed.

Optical Lithography

Despite the fact that present day 4X/5X reticle fabrication is barely capable of supporting today's 0.35μm geometries (Fig. 1), there appears to be little doubt that optical lithography will be extended to the 130nm device generation.

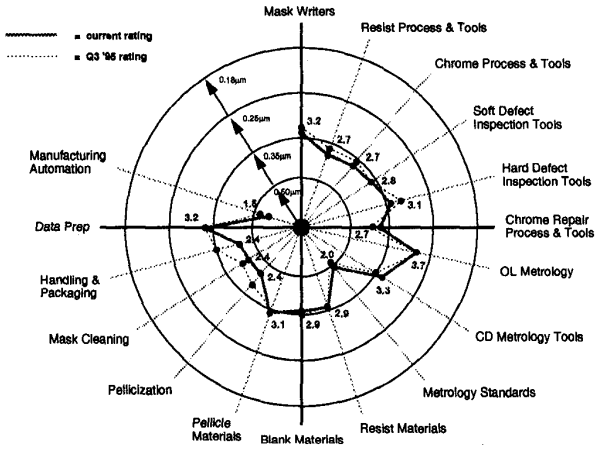

Fig. 1 Spider chart illustrating current reticle capability. Only overlay metrology will support 0.25μm designs.

This is primarily due to evolutionary progress in optical materials and designs, development of high contrast resist processes, and anticipated improvements in reduction reticle technology. However, even with state-of-the-art high numerical aperture (0.6) 193nm optical steppers or scanners, the ratio (k_1) of pattern size to wavelength/NA is less than 0.7 at 225nm feature size. Optical image transfer becomes very non-linear for k_1 below 0.7, requiring design data corrections (OPC) to compensate for such imaging distortions as line end shortening and size differences between isolated and dense lines. More importantly, optical image contrast also begins to decrease for $k_1 < 0.7$, leading to loss in depth of focus, energy latitude and feature size control. OPC and PSM are the primarily optical enhancements used to correct these printing limitations, and both have implications for device design and reticle layout.

Optical Proximity Correction

Fig. 2 illustrates the output of a typical OPC algorithm designed to minimize line end shortening and linewidth variations resulting from optical pattern transfer at k_1 below 0.7. Many serifs and anti-serifs have been generated to improve image transfer fidelity. Unfortunately, this can also result in a significant increase in data volume, over a factor of five in this example. This is turn usually results is very large output pattern files which may require many hours of computation for OPC conversion, particularly for high density device designs containing $>10^7$ transistors. An additional complication is the difficulty of reliably inspecting the corrected mask following insertion of sub-resolution features. At deep sub-micron design rules, reticle resolution

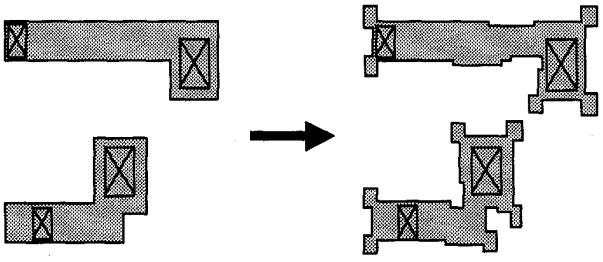

Fig. 2 A typical OPC algorithm converts simple interconnect patterns into a complicated layout in order to compensate for image nonlinearities and loss of high spatial frequencies in optical lithography. Cross-hatched squares are overlying or underlying contacts.

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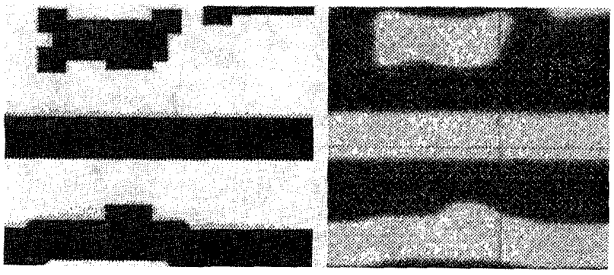
and linearity is a strong function of the writing tool and writing strategy as well as the resist and etch processes used. In addition, there are contrast limitations imposed by the reticle inspection tool. Depending on the balance between required resolution and available reticle technology, all these effects may result in compromised patterns that must be dispositioned during reticle inspection. Fig. 3 illustrates the loss of reticle pattern fidelity that can result from laser pattern generation of 0.25μm 1X features including OPC serifs used to correct for line end pullback. Without adequate compensation built into the reticle inspection strategy, it may not be possible to distinguish real OPC shapes from random defects using high sensitivity inspection thresholds, particularly if inspected in a die-to-database mode (1).

Phase Shift Masks

Increased use of phase shift masks is anticipated as optical lithography is extended to deep submicron dimensions. Both attenuated (weak) and Levenson (strong) PSM techniques are expected to be used to enhance interconnect and conductor patterning, respectively. In the case of attenuated PSM's, pattern data must be modified using either global or selected sizing with no significant change in data volume, or with modified OPC algorithms that in principle add the same data complexity as with OPC-corrected binary masks. However, qualification of such reticles is usually difficult because existing inspection and repair tools are not well matched to the optical and physical properties of attenuated PSM's. Nevertheless, use of i-line attenuated PSM's is increasing worldwide, particularly for memory applications, and is being supported by an expanding infrastructure for reticle blanks, process equipment and design tools.

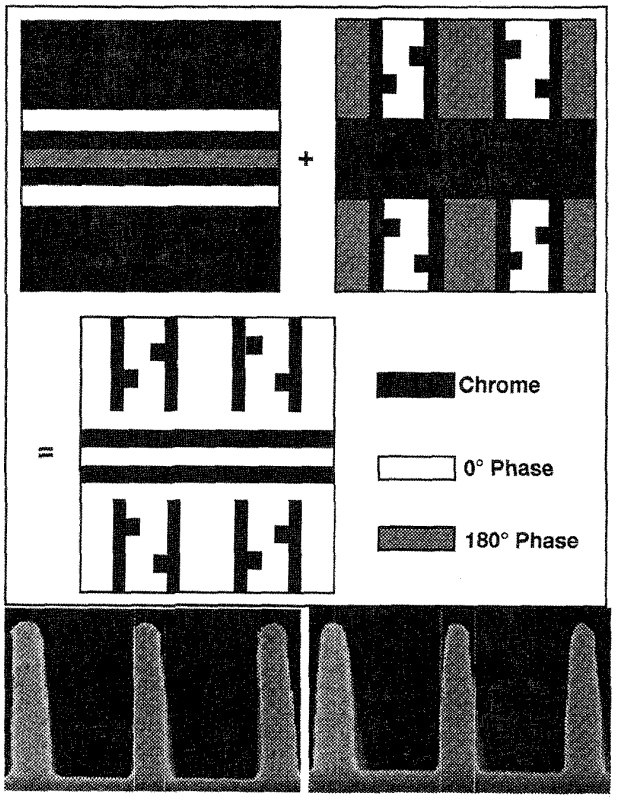
Recently there has also been renewed interest in the use of strong phase shift masks to enhance gate lithography capability, particularly for random logic applications. Because MPU gate requirements are typically 1 - 2 years ahead of the SIA lithography roadmap, aggressive optical techniques are needed to achieve resolution and CD control. Strong PSM's can provide that capability providing a design method can be found to avoid 0°/180° phase conflicts that inevitably arise in any random logic layout. Conflicts may be avoided by using 60° and 120° transition regions between the phase extremes. While this "multi-phase" method has been successfully demonstrated, real estate and defocus margin losses associated with multiple phase transition regions become problems below 1μm pitch, even with DUV lithography (2).

An alternative strong PSM approach makes use of "complementary" masks, illustrated schematically in Fig. 4. using a positive resist process. In this technique all high resolution regions are defined by 0°/180° phase transitions, but phase conflicts are avoided by first building all phase regions within separate dark field blockouts whose boundaries are defined by critical and non-critical edges. Superposition of two exposure fields on the wafer then eliminates unwanted (non-critical) boundaries. This approach



(3a) (3b)

Fig. 3 Optical micrograph (3b) of a 4X reticle produced by a laser pattern generator shows severe loss of OPC resolution compared to the design data (3a).



Focus = -0.4μm Focus = 0.4μm

Fig. 4 Complementary PSM design layout illustrating placement of 08 and 1808 phase regions on a positive tone reticle. Bottom SEM's show DUV printed 100nm resist lines at 0.42μm pitch printed with this technique.

requires excellent overlay between patterns printed with separate reticles or with two halves of the same reticle as well as very precise stepper stages, both possible with state-of-the-art mask technology and exposure tools. In addition, sufficient wafer real estate is required for tolerancing in order to accommodate edge placement errors and unwanted "light leakage" from non-critical boundaries, factors which tend to limit practical complementary mask applications to approximately 0.4μm pitch with DUV lithography. However, design algorithms to generate the necessary complementary regions have been described, as have applications yielding 130nm gates with excellent CD control (3).

Next Generation Lithography

As integrated circuit technology approaches the 100nm generation (100nm lines/spaces for DRAMS, 70nm isolated gates for logic) optical lithography appears to reach its limit, even with the use of OPC and PSM on tools operating at 193nm wavelength. There are multiple technologies competing to demonstrate patterning capability at these dimensions, but none has so far proved this capability convincingly enough to mobilize industry support. However there are efforts underway to assess the technology alternatives. The SEMATECH Program for Next Generation Lithography (NGL) exists to generate a recommendation on the technology path for post-193nm lithography, and to focus global industry resources on that path. There are five technologies being considered, each of which has a unique and daunting set of challenges associated with it. From the designer's perspective, the details of the technology are not as important as an understanding of the data path from design to wafer. This path is different for each technology but some will require more significant changes than others. The options are discussed below.

Extreme Ultraviolet Lithography

The data path for Extreme Ultraviolet (EUV) lithography would be most similar to today's technology, with E-beam writing on masks at 4X the wafer pattern size. However, EUV uses reflective optics in the 10-14nm wavelength range, which means that the optics and the mask must be composed of multilayer stacks (Fig. 5) with up to 40 layer pairs of materials such as Mo/Si or Mo/Be (4). A key technical challenge for this technology is the production and patterning of these mask blanks without defects, since there is no way to repair defects in the multilayer stack. However, the masks would not offer significant difficulties from a designer's viewpoint, as it is likely that OPC will not be needed until at least the 70nm generation. This makes EUV an attractive option, if defect-free blanks and many other technical obstacles related to the tool can be overcome.

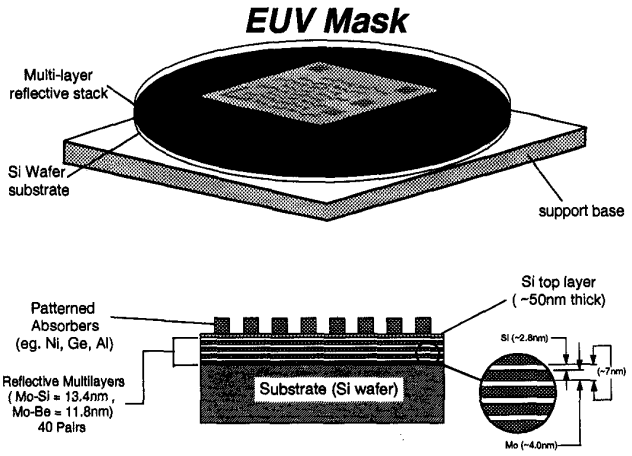


Fig. 5 Schematic view of an EUV mask.

Proximity X-Ray Lithography

Another NGL alternative is Proximity X-ray Lithography, which uses ~1nm light to expose wafers held 10-30μm from a 1X mask. Mask fabrication at 1X is a major difficulty for this technology, and the pattern must be produced with a high aspect ratio in a refractory metal on a 2-3μm thick membrane, typically SiC (Fig. 6). Moreover, it is likely that some OPC techniques will be needed for feature sizes less than 130nm (5). Though the data explosion issue will be comparable to the optical OPC case, patterning and inspection of sub- resolution OPC structures at 1X will be extremely challenging, requiring development of new generation E-beam mask writers capable of extremely precise pattern placement accuracy (<15nm) as well as use of E-beam reticle inspection technology. In addition, the possible need to correct for process-induced mask distortions may complicate pattern data preparation and verification.

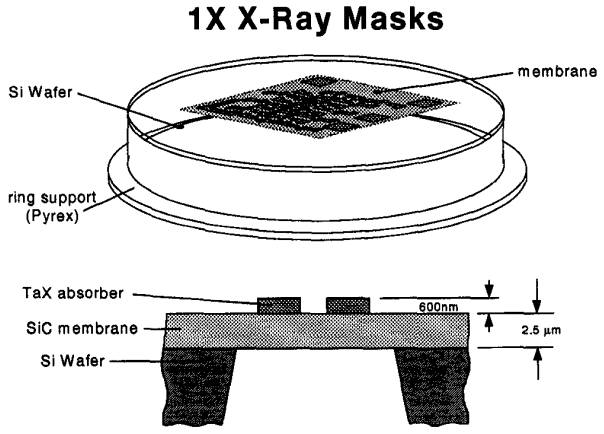


Fig. 6 Schematic view of an X-Ray mask.

Projection E-Beam Lithography

The other NGL techniques require fairly radical departures from conventional pattern transfer onto mask blanks. Lucent's projection E-beam technique, dubbed SCALPEL (**SC**attering with **A**ngular **L**imitation **P**rojection **E**-beam **L**ithography) requires a 30nm thick scatterer layer patterned on a 100nm thick SiN membrane (6). The membrane covers 1mm x 40mm "windows" cut into the backside of a Si wafer, each separated by 100μm wide struts which are required for structural support (Fig. 7). A beam of electrons is projected through the membrane, while the electrons which impact the patterned layer are scattered outside of an aperture in front of the 4X reduction electron optics. The presence of the separate windows on the mask will introduce a new degree of complexity in the data handling. The pattern data will have to be split in such a way that it fits over the windows without any overlap onto the struts. Steps may need to be taken to ensure that features are not split in such a way that small sub-resolution portions are left isolated on the next window over from the main portion of the feature. A key challenge for this technology is the stitching required to recreate a seamless image from the separate windows on the mask. An allowance for stitching errors may need to be built into the data algorithms such that critical features, e.g. microprocessor gates, are not allowed to flow across windows.

Ion Projection Lithography

Ion Projection Lithography (IPL) requires a stencil mask with holes in a 3μm thick Si membrane (Fig. 8). An ion beam is swept across the mask and projected through the stencil pattern and into a 4X-reduction electrostatic column (7). Fabrication of such a stencil mask is challenging enough for whole patterns, but for some layers there will be the additional requirement of producing complementary masks from split pattern data. This is because of the "donut problem" in which certain features cannot be formed using a stencil because they would be free-standing, or nearly so. Even long lines will require separation into segments on complementary masks because of the structural impact of a long stencil hole on mask stability. As with X-ray masks, short and long range pattern-induced mask distortions, as well as possible full field image distortion, must be accurately compensated in order to achieve acceptable pattern placement. Like SCALPEL, this technology also requires accurate stitching, in this case stitching of complementary masks. The separation of the pattern data into complementary masks will require the development of new algorithms that will impact design rules.

Electron-Beam Direct Write Lithography

In the past, the most straightforward data path from design to wafer was associated with Electron-Beam Direct Write Lithography (EBDW), the same technology that is used for photomask manufacturing today. The obvious advantage of conventional EBDW is that there is no mask, but it unfortunately suffers from extremely low throughput, making it impractical for high volume manufacturing. Various approaches have been used to speed up EBDW, the most promising of which is cell projection. Cell projection does result in higher throughput, but introduces a type of mask which mitigates much of the original advantage of EBDW as a maskless technology. Cell projection uses a small Si stencil-mask built into an electron optical column with a reduction factor from 25X to 60X (8). Each stencil mask would be patterned with a "library" of 20 to 30 repetitive structures used in the device (Fig. 9). The size of the stencil pattern segments is determined by the beam size, typically 5μm square. Such a library of structures could be used to expose as much of the chip as could be divided into

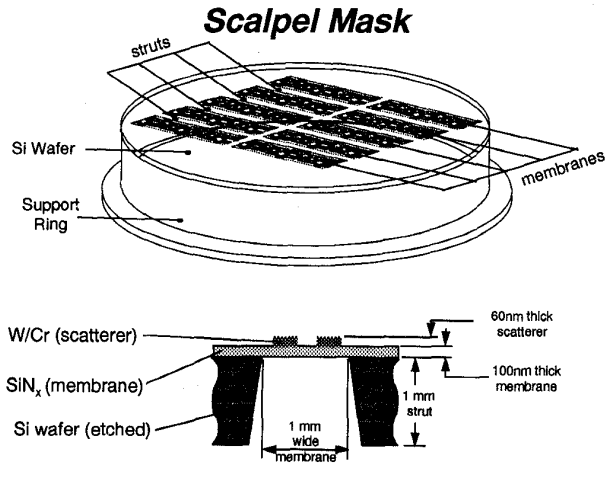


Fig. 7 Schematic view of a SCALPEL mask.

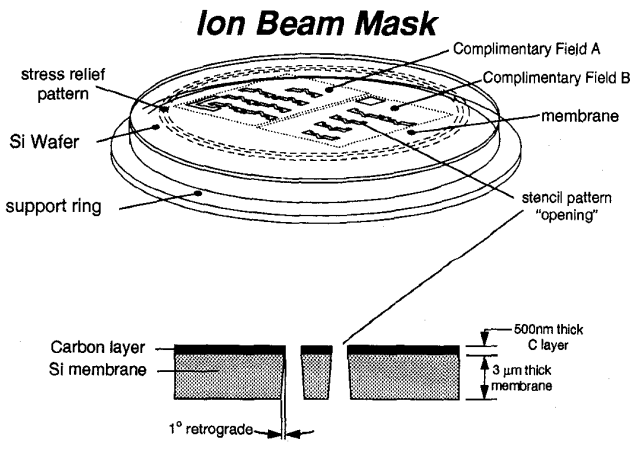


Fig. 8 Schematic view of an IPL mask.

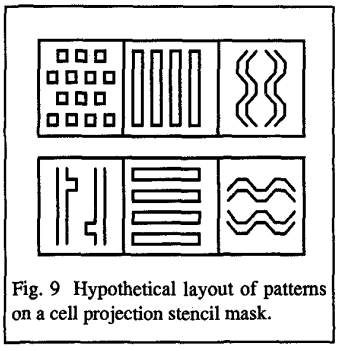


Fig. 9 Hypothetical layout of patterns on a cell projection stencil mask.

these repetitive patterns, with the remainder of the device being exposed directly. Throughput is still considerably lower than with other technologies, but the most benefit would be available for devices that could be constructed as much as possible from the set of stencil-mask patterns, e.g. memory. An interaction between designer and mask maker would be necessary to ensure optimal matching of the stencil mask library to the data set.

Summary

As device dimensions shrink, the current well-developed algorithms for handling pattern data will need to be replaced by new, more complex algorithms capable of handling many times the current data volume. This is becoming evident at the 180nm and 130nm device generations, and will likely become more so as device geometries shrink further. It is a result of the increasingly complex techniques which must be employed by lithographers to reproduce the pattern data accurately on the wafer. In addition, at 100nm and beyond, new post-optical technologies will be required. Several of these technologies will require radical changes in data handling, e.g. support for pattern separation into stripes or complementary patterns. The need for a higher level of complexity and sophistication in the tools which bridge the gap between designers and lithographers is becoming increasingly apparent.

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