An Integrated PLL Clock Generator for 275 MHz Graphic Displays

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Abstract

A monolithic phase-locked loop (PLL) and clock generator/driver has been developed to provide clock frequencies up to 275 MHz from low cost crystals for use with high resolution RAMDACs (random-access-memory and digital-to-analog converter). Unlike previous integrated PLL's, this PLL clock generator simplifies video clock generation design since it requires no coils or varicaps. The internal capacitor for an emitter coupled multivibrator achieves high quality, with little coupling to the substrate. This integrated circuit incorporates all of the building blocks of a PLL, including a crystal amplifier which will work with a wide range of crystal frequencies. The only external components required are two resistors and two capacitors which operate at low loop filter frequencies. An innovative method of efficiently simulating PLL's was also developed.

Introduction

As color display resolution increases the need for inexpensive sources of master clock becomes important. For a 2k by 1.5k pixel display, for example, typical "pixel rate" is 263 MHz. The required jitter specification for this clock is as low as 0.25 nS, and there can be no low frequency periodic disturbances, because they will be visible in the display. It becomes mandatory, unless low price, quality, resonators become available, to use a phase-lock technique to multiply up the frequency of an inexpensive low frequency crystal. The purpose of this project was to develop a monolithic, easy to use, PLL and pair it with all the clocking functions required by today's popular RAMDACs. These clocks are provided by a dedicated combination of ECL logic, for the pixel frequencies, and TTL logic for the control of loading and multiplexing. The design challenge consisted of integrating inherently noisy TTL clock drivers with a sensitive PLL, and required several layout and isolation tricks. The ease of use is related to the absence of external high frequency components; only low frequency loop filter and biasing components are required.

PLL's are traditionally difficult to use because they either require an external VCO, or because the onboard VCO requires external RF components. Controlling the layout of a circuit that oscillates at 275 MHz is far from trivial. And, in general, because of the narrow tuning range of some VCO's, several external components need to be changed to vary the output frequency range. Integrating all of the VCO, at these frequencies, not only makes the PLL less difficult to use, but provides a "black box" solution with ready to use signals. Furthermore, the integrated VCO can have much wider tuning range than the externally tuned types.

Monolithic PLL's have been recently receiving considerable attention. Several papers report work both in bipolar and CMOS processes, and show that this technique is maturing in monolithic form. We believe that the overall performance of our PLL clock driver requires bipolar design. The main limitation of CMOS is in realizing good ECL and TTL output drivers. It also seems that current mode logic of bipolar design is superior in power supply noise rejection.

Functional Description

The integrated phase-locked loop/clock generator consists of a crystal amplifier, a PLL, a voltage reference, and the clock generation functions, as shown in Fig. 1. The crystal amplifier can be used to build a Pierce-type crystal oscillator or it can be driven by an external TTL clock. The PLL consists of a multivibrator voltage controlled oscillator (VCO), a digital phase-frequency detector, a current-out charge pump and an externally programmable divider. The VCO in turn consists of a current controlled oscillator and an operational amplifier connected as a voltage to current converter. The voltage reference of 1.2 volts is available for setting the range of the RAMDAC's converters.

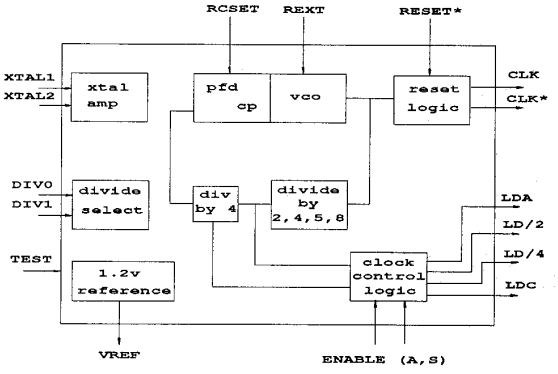

Fig 1. Block diagram of PLL clock driver

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The chip provides all the clock generation functions of similar clock drivers for RAMDAC's. Two of the TTL load clocks are enabled either synchronously or asynchronously and can be used to stop reading the RAM during retrace. A reset pin stops the pixel clock for the number of cycles required to clear a RAMDAC. There is also ld/2 and ld/4 functions of the load clocks which are used for muxing of banks of external video RAM's.

In addition, this clock generator has multiple test modes. For instance the loop can be opened at several places to allow full testability of all the building blocks. Test signals are routed to the blocks under test and their individual responses can be observed. An external voltage source can directly drive the VCO to measure its linearity, power supply rejection, temperature coefficient, or any other function. However, the most comprehensive test for a PLL is to make it lock, since this requires the simultaneous operation of several blocks.

Main Loop Components

The VCO is a standard emitter coupled multivibrator with some enhancements to improve temperature coefficient [1], [2]. The capacitor which determines the frequency range is built with a three layer metal process, with the bottom metal used as a substrate shield. The two top plates make up two capacitors with their electrodes cross connected to further cancel common mode injection [3]. The size of this capacitor in relation to parasitics, and the high linearity voltage to current converter provide a VCO of linear characteristics. An external resistor in the voltage to current converter allows selection of the VCO range. Extended VCO range increases the sensitivity to stray noise, but this is offset by the lower time constant set by the lower external resistor. The observed upper range of the VCO exceeds 450 MHz and scaling down the timing capacitor predicts operation up to 700 MHz. The measured phase noise close to the fundamental is low, which is attributed to the quality and internal location of the timing capacitor.This type of VCO has a wide tuning range and does not require external components like coils or varactors.

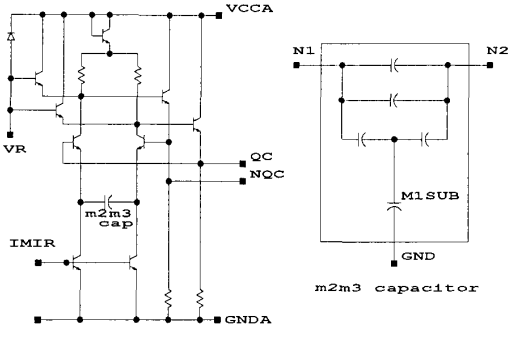

Fig 2. VCO schematic

The charge pump (CP) is an I-2I design. Only NPN transistors switch sinking currents off and on. Slow PNP transistors make up the fixed sourcing current. The switching transients are controlled to provide matched rising and falling times in the output pulse. As shown in Fig. 3, the current sources are mirrored from the PNP to the NPN side to achieve matching. When the PLL is locked, only one NPN source is on and no net current flows out of the chip. The bandgap voltage reference for these is designed to offset the dynamic temperature coefficient in the charge pump. A mismatch of the current sources results in leakage into the external loop filter, requiring periodic corrective pumping. Worse than just creating a small phase offset, the periodic pumping may cause the VCO to produce a frequency modulated output, with phase error drifting out of specification between corrections. The instant the charge pumps, a jitter is also produced in the pixel clock, due to the "zero" in the loop filter. Because of the loop divider, the jitter is observed every N cycles of the pixel clock, where N is the divide ratio. All these effects are reduced by current matching and by the selection of large loop integration time constant.

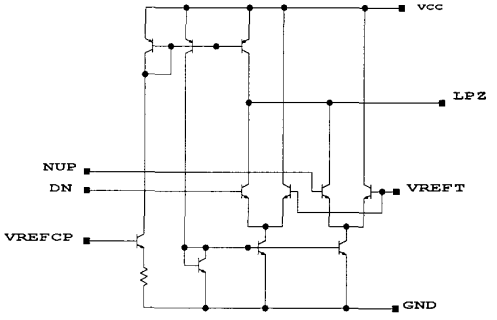

Fig 3. Charge Pump schematic

The crystal amplifier was selected to give optimum performance in terms of frequency offset, bandwidth, biasing and ease of use [4]. It is basically a linear amplifier of fixed gain and known input and output impedance. The amplifier has been made to oscillate with crystal frequencies from 3 MHz to 27MHz, which shows it has a good gain-bandwidth product.

Transient Simulation

We used HSPICE to simulate the transient operation of the PLL. The loop building blocks are all converted to operate on phase, which prevents having to have oscillators. As shown in Fig. 5, a subtractor, a divider, and an integrator were required, and were built up from combinations of controlled sources [5]. The integrator, for instance, is made up of a VCVS (voltage controlled voltage source) driving a 1 ohm resistor in series with a 1 farad capacitor. We refined our simulation by adding an approximation to a digital phase frequency detector. Since under lock the charge pump feeds very narrow impulses, we can approximate it as a narrow amplitude modulated pulse [6],[7]. The voltage

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control resistor (vcr) is switched by a narrow pulse at the expected lock frequency. It transfers, through the VCCS, an amount of charge proportional to the phase difference, and this goes to the loop filter. We verified the predicted stability for a time discontinuous loop in this way. Note that one can easily add parasitics and non-linearities to the simulator.

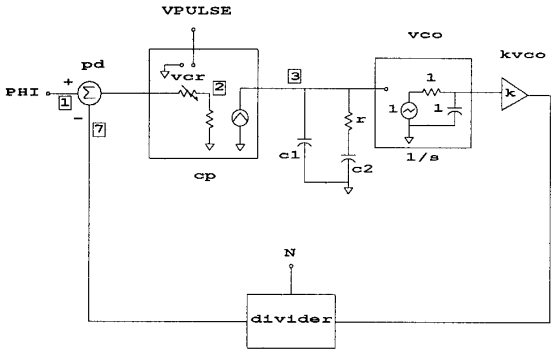

Fig 4. Transient simulation model

The simulator helps develop a "feel" for the stability of the PLL. We used the option "sweep" to verify operation over several ranges of loop components, divide ratios, VCO gains and lock frequency. Figure 5 shows a family of curves where we are varying the N, the divide number, at values of 16, 24 and 32. The next figure shows, form top to bottom, the input and feedback phase waveforms, at the input to the subtractor (pd), the impulse-like phase error, at the output of sampler (cp), and the loop filter voltage.

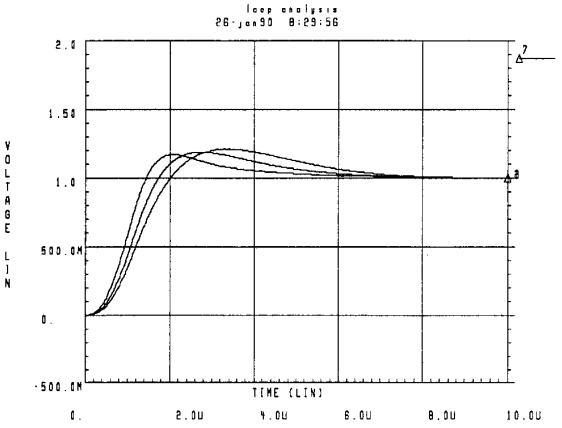

Fig 5. Family of curves for varying N

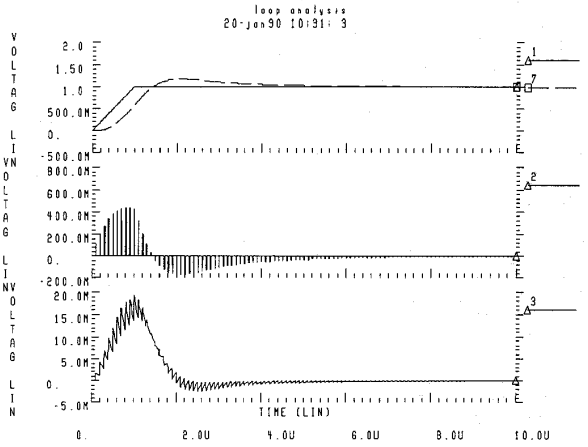

Fig 6. Details of transient simulation

Layout

The VCO and the output buffers were laid-out on opposite sides of the chip and run from separate power supplies. Substrate contacts surround the VCO and isolate it further. The digital side is divided into the noisy output buffers and the core logic. The output buffers are also shielded by a substrate contact barrier.

The chip is shown in the photograph in figure 7. The upper right corner holds the on board timing capacitor and VCO. The left side contains the output buffers. The bipolar process which produced this part has an ft of 6 GHz, and uses lateral pnp structures, schottky diodes, and a three layer metal system. The third layer of metal is very useful both for making the die smaller and for improving analog performance.

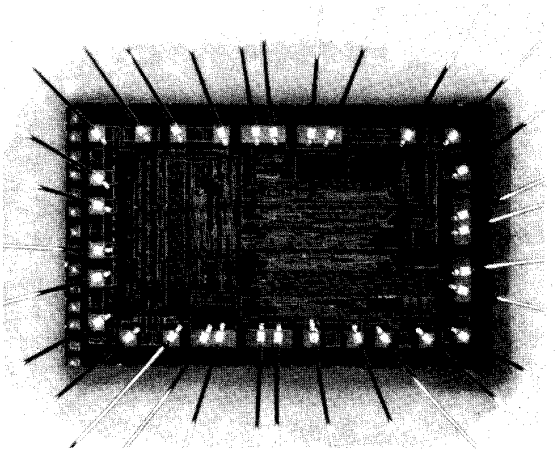

Fig 7. Photograph of PLL clock driver

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Measured Results

A typical range of frequency over which the PLL will lock, without changing the external resistor, is 80 MHz to 275 MHz. This is a wide range and it allows the users a lot of flexibility in clock frequency selection without component changes. We have measured good phase noise without isolating the analog ground, using a single 5 V supply with local decoupling networks. Supply noise rejection was measured at 1 Vpp up to 10 KHz. Low power consumption of 800 mW maximum permits using a 28 pin PLCC package for smaller board space. This part has been demonstrated driving a 1280 by 1024 display with no observable pixel jitter or low frequency wandering of the screen. The photograph shows the pixel clock locked at 256 MHz and one of the TTL load clocks. The input crystal was 8.0 MHz and the divide ratio 32. For the middle range of graphic display frequencies we find crystals of around 10 MHz to give most flexibility and higher performance. This is related to the choice programmable divide ratios and the size of external capacitors required to resonate the lower frequency crystals.

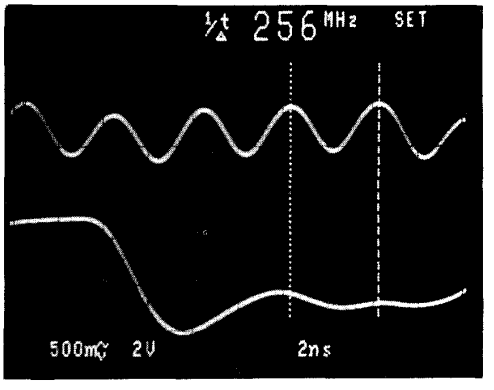

Fig 8. Pixel clock and one load clock

Conclusion

We have shown a single chip PLL clock driver for high resolution graphic displays, which operates in excess of 275 MHz and is easy to use. One direction to optimize the design will be to trade speed for power consumption. We can predict similar performance at half the power, or twice the present speed, after circuit optimization. Another area of circuit improvement is temperature coefficient and voltage sensitivities, in particular to apply the PLL technology to more general uses like clock recovery and signal demodulation. Edge control of fast output drivers will reduce radiation, which, in some environments, can result in no-lock conditions; an improvement here would make the PLL less sensitive to PCB layout.

Several variations of this part are under development. More intelligence in the control of timing, synchronizing and deskewing are being added. This PLL technology breakthrough is broad enough that it will also be incorporated in future ATE and Imaging products.

Acknowledgements

This project was jointly developed by Quadic Systems, which provided PLL experience, and Brooktree, which carried out resimulation and chip integration. Credit is due to Bryan Peter and Benny Chang, of Quadic Systems, who designed the VCO and Crystal Amplifier, respectively, and developed simulations and outstanding documentation.

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