STEPPED-ETCHING FOR PRESERVING CRITICAL DIMENSIONS IN THROUGH-WAFER DEEP REACTIVE ION ETCHING OF THICK SILICON

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ABSTRACT

This paper presents the experimental investigation of stepped deep reactive ion etching (DRIE) process in order to minimize critical-dimension (CD) variations due to local heating observed in through-wafer etch of 100µm-thick, high aspect ratio silicon microstructures that are suspended over glass substrate. Classical methods of cooling the substrate, using a heat-sink layer, or increasing the thickness of sidewall passivation in general turns out to be insufficient for preventing excessive damage in critical dimensions during deep etches. Alternatively, stepped etching is evaluated for improving the CD variation in deep through-wafer etch. Preliminary results indicate that the CD variation improves from +2.56µm to +0.55µm for a 2µm-wide and 100µm-deep capacitive comb finger gap, by using 7 successive DRIE steps with 10min etch and 20min interrupt periods, compared to a single 70min DRIE without any interrupt.

KEYWORDS

Deep reactive ion etching (DRIE), high-aspect ratio micromachining, DRIE heating effect.

INTRODUCTION

Heat induced over suspended silicon structures during etch is transferred to the cooled substrate through narrow trenches until these trenches are completely etched. Once non-critical wider trenches are etched through, the entire thermal load is then carried by critical structures with minimum trench gaps, resulting in local heating around them [1]. Cooling the substrate is observed to be insufficient for controlling this local heating, since the thermal conductance of critical structures significantly decrease towards the end of the etch and become a limiting factor in heat transfer. As a result of limited heat conduction, significant CD variations are observed in deep through-wafer etches by increased sidewall etch rate. One solution to this problem is proposed as coating a sacrificial metal layer under silicon, acting as a heat sink throughout the etching [2, 3, 4]. However, the thickness of this metal layer is usually in sub-micrometer range, and therefore, it cannot always act as an effective heat sink under the 100µm-thick silicon. Another solution is to play with DRIE process parameters during etch [1, 5], which will only work for some small-area suspended structures and for a limited etch period.

This research is based on a simpler and more generalized method of applying a step-by-step through-wafer etch instead of a one-time etch, allowing the critical structures cool down to the substrate temperature within the etch interrupt periods.

THROUGH-WAFER FABRICATION PROCESS

The fabrication process is based on silicon-on-glass micromachining [3], while interconnect and pad metallization is patterned over the glass substrate instead of silicon as in [3]. Figure 1 shows the process flow, on which this etch optimization study is conducted. Process starts with anchor formation on a 500µm-thick glass substrate followed by patterning of Cr/Au interconnect metallization. Next, a thin Cu or Al shield metal is patterned at the bottom of the thin silicon substrate, which will act both as an etch-stop layer for through-wafer DRIE and a heat-sink. After anodically bonding the silicon and glass substrates, the silicon is through-wafer etched using DRIE until reaching the metal etch-stop layer. Finally, the etch mask for DRIE and the etch-stop layer are removed and the structures are released following an alcohol rinse.

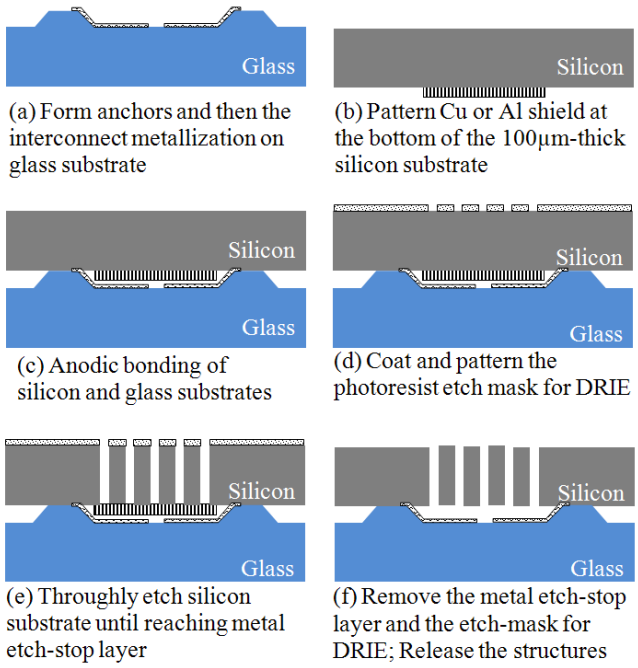
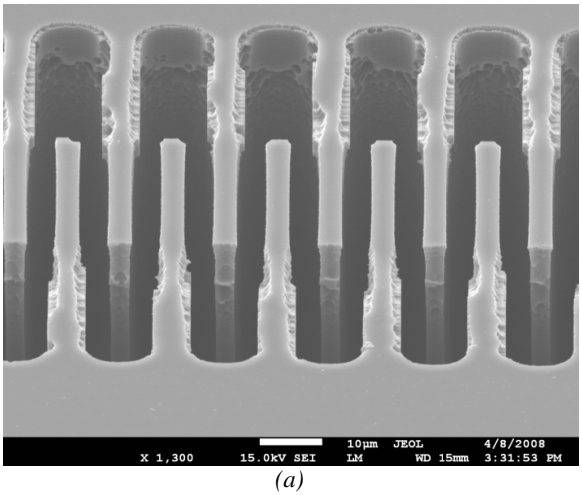


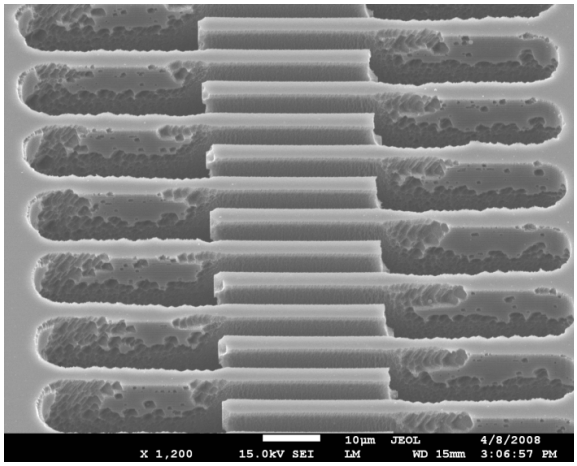
Figure 1: Process flow for through-wafer etching of silicon.

LOCAL HEATING OBSERVED IN CRITICAL MICROSTRUCTURES

Process flow of Figure 1 is straightforward until through-wafer etching of the 100µm-thick silicon substrate (Figure 1-e). This etching step, however, requires additional care as it directly determines the variations in the critical dimensions of suspended silicon structures. Figure 2 shows the SEM pictures of the capacitive comb fingers through-etched by DRIE within 70min without any interrupts. Here, the width of the capacitive gap is measured to be 4.56µm at the trench top, corresponding to a CD enlargement of 128% considering the nominal layout value of 2µm. The lithography step for patterning the DRIE etch mask is responsible only for 0.2µm of the observed CD variation. The remaining part is determined by DRIE and basically dominated by local heating of suspended silicon structures during etch.



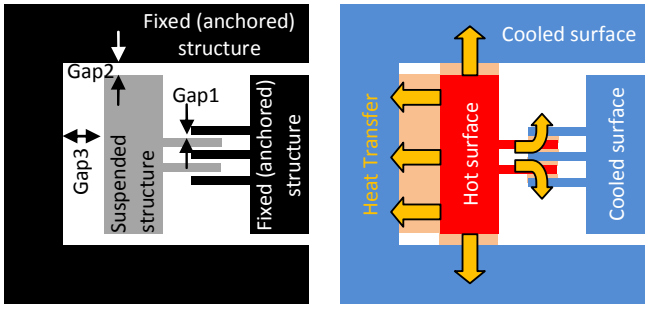
(a)



(b)

Figure 2: SEM pictures of the capacitive comb fingers throughly-etched by DRIE within 70min without any interrupts. (a) Capacitive gaps are enlarged to about 4.5µm from 2µm layout value. (b) Excessive deformation of sidewall passivation.

Figure 3 illustrates the local heating problem that face suspended silicon microstructures during DRIE through-wafer etch by showing the conceptual variation of thermal cooling paths in time for these critical structures. The variation of thermal cooling paths is a result of aspect-ratio dependent etch (ARDE) in DRIE [6], which results in the fact that the smaller openings are etched in a longer period of time. On the other hand, maximizing the sensitivity of capacitive sensors requires the use of minimum-size capacitive gap opening and minimum comb width, i.e., being the critical dimensions of the sensor. These critical structures remain as the only thermal paths towards the end of DRIE through-wafer etch, for cooling some large-area suspended silicon structures attached to them. This phenomena result in local heating of critical structures, which cause significant CD and performance variation for the fabricated capacitive sensor structures [3]. Dividing a long through-wafer etch process in shorter and successive etching/cooling steps can significantly reduce the deformations due to local heating, which is experientially verified and the results presented in the next section.

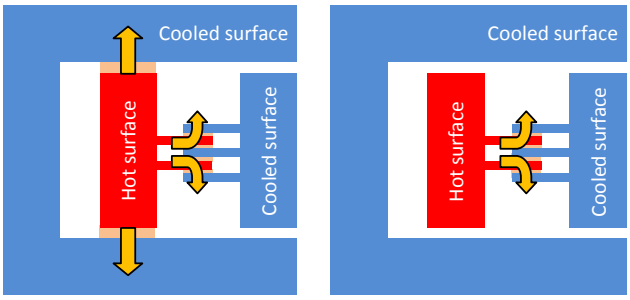


t=0
Gap1<Gap2<Gap3
Gap1: Critical dimension

(a)

t=(1/4)*t_{etch}
Heat transfer through Gap1, Gap2, and Gap3

(b)



t=(2/4)*t_{etch}
Gap3 completely etched.
Heat transfer through Gap1 and Gap2 only

(c)

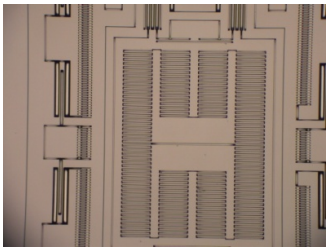
t=(3/4)*t_{etch}
Gap2 and Gap3 completely etched.
Heat transfer through Gap1 only.
Local heating around Gap1

(d)

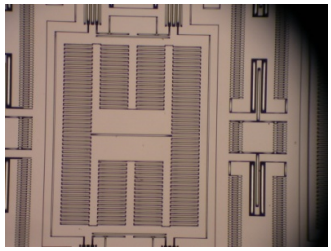
Figure 3: Illustration of local heating problem and the conceptual variation of thermal cooling paths in time for suspended silicon microstructures. The time variation of thermal paths closely depends on the mask layout.

EXPERIMENTAL RESULTS FOR STEPPED THROUGH-WAFER ETCHING

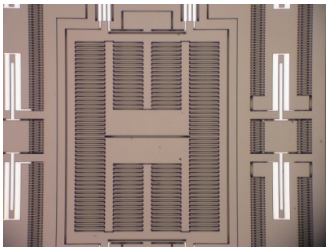
Figure 4 shows the results of a stepped through-wafer etch applied on an inertial sensor prototype. The process consists of 7 DRIE steps each being 10min long and having 20min post-etch interrupts. It is observed that 20µm openings are through-etched within 40min, while it takes 50min, 60min, and 70min for the etch to be completed in 10µm, 3µm, and 2µm wide trenches, respectively, due to aspect-ratio dependent etch (ARDE) characteristics of DRIE [6].



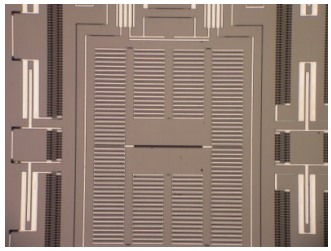
(a) After 20 min etch. No open trench.



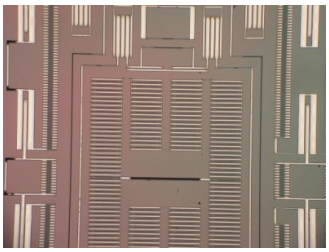
(b) After 30 min etch. No open trench.



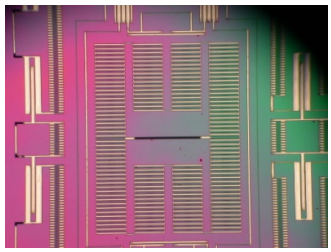
(c) After 40 min etch. 20µm trenches open.



(d) After 50 min etch. 10µm trenches open.



(e) After 60 min etch. 3µm trenches open.



(f) After 70 min etch. 2µm trenches open.

Figure 4. Results of a stepped through-wafer etch applied on an inertial sensor prototype. Process consists of 7 DRIE steps each being 10min long and having 20min post-etch interrupt.

Figure 5 shows the variation of normalized thermal conductance of suspended silicon frame on which the comb fingers with critical dimensions are attached. The ARDE effect complicates the stepped-etch optimization, since the total thermal resistance and resulting local heating associated with suspended structures increase significantly as the etch proceeds towards the end.

Figure 6 verifies this hypothesis by showing close-up pictures of the comb fingers after the last four etch steps, indicating that severe sidewall destruction occurs within the last etch step as the thermal load on the comb fingers significantly increases after 60min etch.

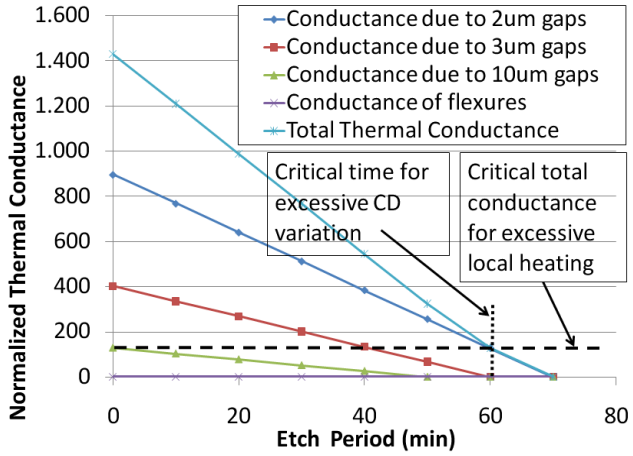
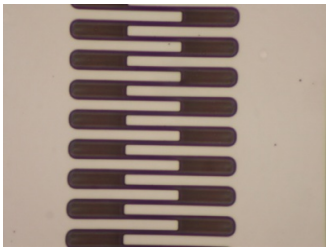
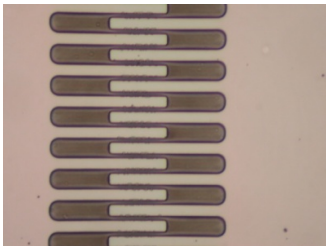


Figure 5. Variation of normalized thermal conductance of suspended silicon frame on which the comb fingers with critical dimensions are attached



(a) After 40 min. No sidewall destruction.

(b) After 50 min. No sidewall destruction.



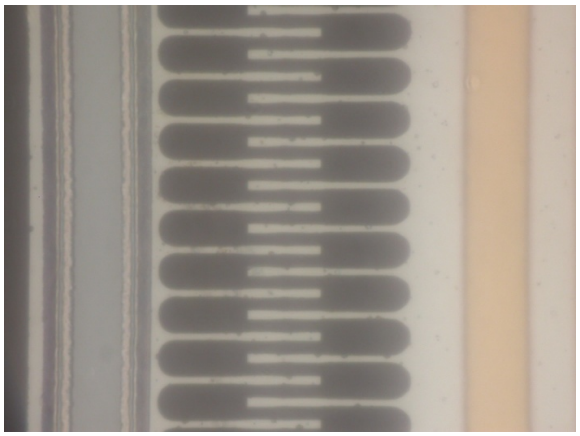
(c) After 60 min. Slight sidewall destruction.

(d) After 70 min. Severe sidewall destruction.

Figure 6: Close-up photographs of the comb fingers (photoresist etch mask not stripped) within the last 30min of the etch following a 40min stepped DRIE, indicating that severe sidewall destruction occurs within the last etch step as the thermal load increases on the comb fingers.

Figure 7 shows the nominal 2µm-wide comb gap, which is enlarged to 2.55µm from the top after 7x10min stepped-etch corresponding to a CD enlargement of only 27.5%, i.e., about 5 times better than what has been achieved with single 70min DRIE without any interrupt. The average gap width is 3.46µm corresponding to an aspect ratio close to 30 with a profile angle of 89.5°.

(a) Top side after 70 min. Capacitive gap: 2.55μm



(b) Bottom side after 70 min. Capacitive gap: 4.36μm

Figure 7: The nominal 2μm-wide comb gap is enlarged to 2.55μm from the top after 7x10min stepped-etch corresponding to a CD enlargement of only 27.5%, about 5 times better than what has been achieved with single 70min DRIE without any interrupt. An average aspect ratio close to 30 is achieved with a profile angle of 89.5°.

CONCLUSIONS

Preserving the critical dimensions in through-wafer deep reactive ion etching of thick silicon microstructures requires sufficient cooling of the substrate during the etch. This is simply because of the fact that the thermal conductance required for cooling large-area suspended silicon structures significantly reduces during the etch, resulting in local heating around the remaining thermal conductance paths. In general, these remaining paths consist of some critical structures either with minimum spacing or feature size, such as comb capacitors or flexure beams. The method proposed in this paper against local heating is to perform a stepped-etch process consisting of multiple etch steps, the period of each step being shorter than the required total etch period, while sufficient cooling periods are inserted between successive etch steps.

Experimental verification of the proposed method is performed on sensor prototypes fabricated using an in-house silicon-on-glass fabrication process. It has been observed that a 2μm capacitive gap enlarges to more than 4.5μm, indicating a CD enlargement greater than 125%, during a 100μm deep through wafer etch performed by a single DRIE step of 70min long. On the other hand, the same sensor structure etched with 7 successive DRIE steps each 10min long and interrupted by 20min long cooling steps resulted in the same capacitive gap size being enlarged to only about 2.5μm, corresponding to a CD enlargement of about 25%.

In summary, stepped etching improves the cooling of critical structures during a through-wafer etch process. On the other hand, it may be considered to reduce the period and increase the number of etch steps towards the end of a deep etch, for further reduction in CD variation and successful fabrication of very high aspect ratio suspended microstructures by deep through-wafer etching.

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