SILICON NANOWIRE PHOTOVOLTAICS

D. Tham, J. R. Heath
Division of Chemistry and Chemical Engineering
California Institute of Technology, Pasadena, CA 91125

ABSTRACT

Arrays of hundreds of parallel silicon nanowire p-n junction diodes, 20 nm in diameter and separated from each other by 14 nm, were fabricated using a variant of nanoimprint lithography. Bulk film diodes were also fabricated adjacent to the arrays as controls. Dark I-V curves from the nanowire arrays and bulk films suggest that performance is currently limited by surface states.

INTRODUCTION

When bulk photovoltaics absorb light above the band gap energy, excess photon energy above the band gap energy is wasted as heat when photoexcited carriers collide with the crystal lattice in carrier-phonon scattering events. Without carrier thermalization is therefore mainly responsible for reducing limiting efficiencies from the maximum limit of about 68% under unconcentrated sunlight for an infinite tandem cell [1-3].

While spectrum-splitting and tandem cells offer means to mitigate thermalization losses, they generally suffer from increased cost and complexity. Therefore, these advanced designs have not found widespread application except in niche areas where the additional cost can be justified. Consequently, the c-Si PV cell, with its combination of good efficiency at moderate cost, remains the dominant technology in the solar cell market.

In many ways, silicon is an ideal photovoltaic material, because of its low cost and abundance in the Earth's crust, the excellent properties of the interface with its passivating oxide, and decades of experience with its use in the microelectronics industry. Our excellent understanding of silicon's material properties, and our ability to finely manipulate them, also make silicon an ideal system to test ideas for increasing the limiting efficiencies of solar cells. Of those ideas, the concept of the hot-carrier solar cell [4, 5] is most relevant to our experiments.

In the hot-carrier solar cell concept, the carriers are assumed to be equilibrated amongst themselves but are prevented from thermally equilibrating with the lattice, and consequently do not convert the excess photon energies into lattice vibrations. These "hot carriers" have excess kinetic energies representative of an equilibrated carrier population at elevated temperature, which may be exploited by collecting the hot carriers through special contacts [6], or used to generate additional electron-hole pairs via impact ionization [5, 7].

Unfortunately, no known bulk materials exist where the carriers are thermally decoupled from the lattice. Instead, low-dimensional nanostructures have been proposed as possible hot-carrier solar cell materials [8], in part because it appears possible in very small structures to reduce the carrier collection times sufficiently to avoid thermalization [9]. Low-dimensional nanostructures also offer the possibility of improved efficiencies through control of the carrier-phonon interaction via phononic engineering [8].

Recently, our group has discovered a larger-than-bulk thermopower in silicon nanowires, due to a enhanced phonon drag contribution [10]. We believe that phonon confinement in the radial direction forces a renormalization of bulk modes into novel one-dimensional hybrid phonon modes that incorporate the nanowire boundaries. These new modes do not "see" or scatter off the nanowire sidewalls, but instead are limited by the length of the nanowires. Consequently, they have enhanced lifetimes, and the carrier-phonon scattering dynamics are thus different than the bulk. Inspired by this result, we propose that silicon nanowires can serve as an ideal model system to investigate phonon physics in the context of photovoltaic applications.

EXPERIMENTAL PROCEDURE

Patterned Doping

Silicon-on-insulator (SOI) wafers (Ibis Technology) with ~40 nm top silicon layers were cleaved into 1"×1" square chips. Alignment marks were then etched into the SOI wafers using standard optical lithography. The wafers were then cleaned using a standard RCA cleaning protocol.

In a process we call patterned doping which we will describe briefly in the following [11], we used spin-on-glass (SOG) layers as diffusion barrier masks to dope lithographically-defined regions on silicon-on-insulator (SOI) chips with *p*- and *n*-type spin-on-dopants (*p*- and *n*-SOD). Undoped SOG (Honeywell Accuglass 214) was spun onto cleaned wafers on a commercial spinner system (Headway Research). The wafer was then heated to drive off remaining solvent on a hotplate and photoresist was then spun on. Dopant windows were then aligned to the etched alignment marks and exposed using photolithography. The exposed pattern was then developed to expose the underlying SOG through the patterned windows.

978-1-4244-1641-7/08/$25.00 ©2008 IEEE

The wafer was then dipped in buffered oxide etch to transfer the window pattern into SOG, and expose the underlying silicon substrate. Residual photoresist was removed in acetone, and the wafer was then RCA cleaned. Then *p*-SOD (Filmtronics Boron-A) was spun on and dried on a hotplate. The wafer was then loaded into a rapid thermal processing (RTP) system and annealed under nitrogen. A variety of anneal temperatures and times were attempted. After cooling, the wafer was retrieved from the RTP and sonicated in BOE in the dark in 30 s cycles until hydrophobic, rinsed and dried. Rinsing with acetone, methanol and water help the chip surface become hydrophobic, perhaps by removing surface hydrocarbon contamination released during SOG etching. Usually, one or two BOE sonication cycles were required before the surface turned hydrophobic.

The wafer was then RCA cleaned and the *n*-type doping performed using *n*-SOD (Emulsitone phosphorosilicafilm:methanol = 1:10). Identical steps were followed to dope the wafers in separate *n*-type windows. After patterned doping was completed, *p*- and *n*-type regions are side-by-side on the silicon layer and in electrical contact.

Etch Mask Fabrication

We used the superlattice nanowire pattern transfer (SNAP) technique [12] to deposit parallel arrays of platinum nanowires over the pattern-doped regions, which serve as etch masks in a later reactive ion etching step. SNAP imprint masters were cleaved from a wafer with a 400-period MBE-grown GaAs/$Al_xGa_{(1-x)}As$ repeating superlattice (IQE Ltd). After cleaning of the imprint masters, they were etched selectively to expose a comb of AlGaAs ridges. A thin layer of platinum was evaporated obliquely onto the structure to form an array of 400 platinum nanowires along the comb tips. With SNAP, the periodicity of the GaAs/AlGaAs superlattice grown with molecular-beam epitaxy (MBE) is thus translated into a periodic array of platinum nanowires.

To transfer the platinum nanowire array onto the SOI chips, a drop of a dilute epoxy/PMMA solution in chlorobenzene was spun onto prior pattern-doped SOI chips. The SNAP masters were aligned and dropped into pattern-doped regions using a home-built aligner. The wafers with the SNAP masters were then heated to bond the masters to the SOI chip. The GaAs/$Al_xGa_{(1-x)}As$ SNAP masters were etched away in a dilute H_3PO_4/H_2O_2 solution overnight, releasing the platinum nanowire arrays onto the SOI surface.

Additional platinum etch masks for monolithic contacts and bulk film devices were patterned with standard electron-beam lithography and platinum evaporation [13]. EBL was used to pattern larger silicon monoliths for electrical contact to the nanowires, as well as bulk film devices as experimental controls. We employ monolithic contacts primarily to reduce contact resistances [13] to our devices which are detrimental to photovoltaic performance. After metal liftoff, the resulting chips contained platinum etch masks defining the monolithically-contacted platinum nanowire devices adjacent to identically-sized bulk film devices.

Pattern Transfer Into Silicon

The chips were loaded into an RIE system and etched using a CF_4-based plasma, using a reflectivity sensor to monitor the etching process. The etch process was terminated once the buried oxide interface was exposed, resulting in a 1-to-1 transfer of the platinum patterns into the top silicon layer. The chips were then placed in aqua regia to dissolve the platinum etch masks, then rinsed and dried. Standard photoresist strippers (Baker ALEG) were helpful in removing residual polymeric residues from the RIE etch.

At this point, multiple devices on the chip were still electrically connected to each other and so a final etching step was needed to sever these connections. Standard EBL and aluminum evaporation were used to define a new set of etch masks, and the chip was then RIE-etched with an SF_6-based plasma to remove intervening silicon areas between devices. The aluminum masks were then removed with PAE aluminum etch, then rinsed and dried. To remove polymeric residues from the RIE etch, the chip was then heated briefly in PRX-127 resist stripper, followed by rinsing and drying.

Electrical Contacts

Standard EBL was used to write the patterns for the metal electrodes. Large contact pads were written over the monolithic silicon regions to utilize the maximum area for the contacts and reduce contact resistance. After resist development and gentle RIE descumming, the chip was dipped for about 5 s in a dilute BOE solution to remove native oxide over the monolithic silicon regions before electrode deposition. After rinsing with DIW and drying, 20 nm of titanium followed by 120 nm of platinum were evaporated as inner electrodes to the devices. Metal liftoff was performed by soaking in acetone for about an hour.

A second, larger set of contact pad patterns were exposed in registry atop the smaller titanium/platinum electrodes using standard optical lithography. After development and descumming in an O_2 plasma, 200 nm of gold was evaporated onto the chip. Liftoff of the gold contact pad patterns was performed overnight by soaking in acetone. After liftoff, the gold contact pads were wire-bonded to chip carriers for I-V measurements.

Electrical measurements

A digital sourcemeter (Keithley 2400) was used to measure I-V characteristics of the fabricated devices. For two-point measurements of the diodes, voltage was sourced and current measured. For four-point

978-1-4244-1641-7/08/$25.00 ©2008 IEEE

measurements of bulk film and nanowire resistivities, current was sourced between the outermost electrodes and sensed between inner electrodes. All measurements were performed under vacuum and in the dark within a Janis Research ST-100 continuous flow cryostat.

RESULTS AND DISCUSSION

Using the experimental procedure outlined above, we have successfully fabricated several device sets. Each device set contained a nanowire *p*-*n* junction array, with a *p*-type nanowire array and an *n*-type nanowire array on either side. Adjacent to the nanowire devices, a bulk film *p*-*n* junction was similarly flanked by *p*- and *n*-type bulk films. A color-coded SEM image of a typical device set is shown in Fig. 1a. The upper row are bulk film devices, while the lower row consist of nanowire devices. Here red regions are *n*-doped, blue regions are *p*-doped and metal electrodes and contacts are colored green. Fig. 1b is a higher magnification SEM image of the nanowire *p*-*n* junction array, highlighting the excellent quality of the nanowires obtained using the SNAP process.

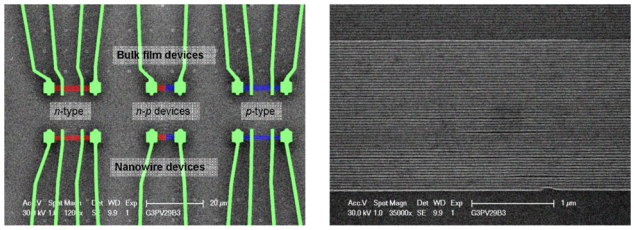

Figure 1. (a) Color-coded SEM image, where *n*-doped regions are red, *p*-doped regions are blue, and electrodes and contacts are green. The upper and lower rows contain bulk film and nanowire devices, respectively. The *p*- and *n*-type bars flanking the *p*-*n* junctions were used for four-point resistivity measurements to estimate effective dopant levels. (b) Magnified SEM image of the nanowire *p*-*n* junction array, with ~20 nm diameter nanowires separated by ~14 nm gaps.

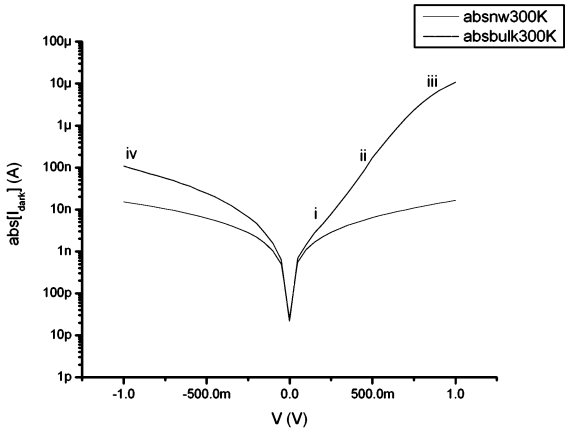

Figure 2. Two-point, dark I-V measurements at 300 K for a typical device set, plotted on an absolute logarithmic scale. The bulk film results are in blue, while the nanowire array results are in red.

Dark two-point diode I-V measurements at 300 K for one typical device set are shown in Fig. 2. The bulk device behaves as expected for a diode, while the nanowire device remains highly resistive. Here the bulk device exhibits hallmarks of the standard diode I-V trace:

(i) space-charge region (scr) recombination at low bias;
(ii) quasi-neutral region (qnr) recombination at higher bias;
(iii) series resistance effects at high forward currents; and
(iv) current saturation at reverse bias.

On the other hand, the nanowire device exhibits little rectification. To understand this behavior, two- and four-point resistivity measurements were performed on the *p*- and *n*-type bars (not shown) to estimate the sheet resistivities on both sides of the *p*-*n* junction. For the bulk films, both *p*- and *n*-type bars produced ohmic, linear I-V traces with low resistance typical of highly-doped silicon with low contact resistances. For the nanowire arrays, the *p*-type bars were highly-conductive, with ohmic, linear I-V traces comparable to the p-type bulk film. On the other hand, the I-V traces from the *n*-type nanowire arrays were typically highly resistive and nonohmic.

We believe that poor *n*-type nanowire conductivities are responsible for poor rectification in these nanowire diodes. While we have not yet obtained ohmic conductivities in *n*-type nanowires, we have observed that the nanowire diode rectification performance improves in device sets with more “ohmic” and less resistive traces. Surface states in our nanowires probably trap a large number of carriers of both types, causing dopant impurities to become electrically inactive [14]. The surface traps in question are probably more destructive to *n*-type conduction than they are for *p*-type, since we always observe this reduction in conductivities with *n*-type nanowires.

CONCLUSIONS

Nanowire array and bulk film *p*-*n* junction diodes were fabricated on SOI wafers, and their dark I-V response was measured. The bulk film junctions were found to perform as expected, but the nanowire diode arrays were highly resistive with low rectification. Four-point resistivity measurements suggest that poor conductivity in *n*-type nanowires was responsible for lack of rectification in nanowire junctions. The cause of the poor conductivity is presumably related to surface traps that are present in our devices. We are presently working on process optimizations to reduce the number of these surface states.

ACKNOWLEDGEMENTS

DT gratefully acknowledges funding from MITRE Corporation (Contract No. 67233), MIT MSD (Contract No. 5710001623) and support by the KAUST Scholar Award.

978-1-4244-1641-7/08/$25.00 ©2008 IEEE

DT also thanks A.I. Boukai and G. M. Kimball for wonderful extended discussions.

REFERENCES

[1] P. Würfel, Physics of Solar Cells, Wiley-VCH, Berlin, 2005, p. 186.

[2] J. Nelson, The Physics of Solar Cells, Imperial College Press, London, 2003.

[3] M. A. Green et al., "Very high efficiency silicon solar cells - science and technology", *IEEE Transactions on Electron Devices* **46** (1999) 1940.

[4] R. T. Ross, A. J. Nozik, "Efficiency of hot-carrier solar energy converters", *Journal of Applied Physics* **53** (1982) 3813.

[5] P. Würfel, "Solar energy conversion with hot electrons from impact ionisation", *Solar Energy Materials and Solar Cells* **46** (1997) 43-52.

[6] G. Conibeer et al., Selective energy contacts for potential application to hot carrier PV cells, in: 3rd World Conference on Photovoltaic Energy Conversion, Osaka, 2003.

[7] S. Kolodinski et al., "Quantum efficiencies exceeding unity due to impact ionization in silicon solar cells", *Applied Physics Letters* **63** (1993) 2405.

[8] M. A. Green, "Prospects for photovoltaic efficiency enhancement using low-dimensional structures", *Nanotechnology* **11** (2000) 401-405.

[9] M. Neges et al., "Monte Carlo simulation of energy loss and collection of hot charge carriers, first step towards a more realistic hot-carrier solar energy converter", *Solar Energy Materials and Solar Cells* **90** (2006) 2107-2128.

[10] A. I. Boukai et al., "Silicon nanowires as efficient thermoelectric materials", *Nature* **451** (2008) 168-171.

[11] D. Wang et al., "Complementary symmetry silicon nanowire logic: power-efficient inverters with gain", *Small* **2** (2006) 1153.

[12] N. A. Melosh et al., "Ultrahigh-density nanowire lattices and circuits", *Science* **300** (2003) 112.

[13] D. Wang et al., "Two-dimensional single-crystal nanowire arrays", *Small* **3** (2007) 2043.

[14] M.-V. Fernández-Serra et al., "Conductance, surface traps, and passivation in doped silicon nanowires", *Nano Letters* **6** (2006) 2674.

978-1-4244-1641-7/08/$25.00 ©2008 IEEE