Systematic Approach to Ultra-Wideband Low Noise Amplifier Design in CMOS technology

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***Abstract* – A systematic approach to CMOS Low Noise Amplifier design is presented. This Method uses a new input impedance matching technique based on LC Ladder Matching Networks. With This approach a LNA is implemented in ADS2006. Simulations results for 0.13µm TSMC technology shows a very low noise figure less than 1.75dB and power gain up to 20dB in middle frequency. S11 and S22 are less than -7 dB and -10 dB in average respectively. This amplifier consumes only 8.846mw power with 1v supply voltage.**

I. INTRODUCTION

Low noise amplifier is the most important component of the receiver front end, due to the fact that it can determine the total noise figure of the receiver system. Designing this part includes many constraints which make total design challenging. Some of these considerations are low noise figure, sufficient gain without contributing much noise, input and output matching improvement and low power consumption. So a well design for this stage plays an important role in performance of the receiver system. New designs are working in wide and high frequency bands like Ultra Wide Band. Since Federal Communications Commission (FCC) allocated the frequency 3.1GHz-10.6GHz to Ultra Wide Band systems in February 2002, the big problem was lack of a systematic approach for designing LNA. Our purpose in this paper is presenting a systematic procedure for designing Ultra-Wideband low noise amplifier based on mathematical relations.

General structure of the amplifier is discussed in part II. In part III,a new approach is described for input impedance matching of LNA using LC Ladder Matching Networks and source degeneration inductor. output matching is presented in part IV. Simulations results are coming in part V. finally we conclude this paper in part VI.

II. AMPLIFIER STRUCTURE

First we must design the core of the amplifier. At the first sight it seems that using multiple stages will increase the voltage gain and it causes canceling the noise of other stages more. But using several stages will increase power dissipation and consequently total noise figure of the system. So using one amplifier stage which provides suitable gain and occupying minimum space is more preferred. Indeed the gain must not be too high, otherwise the large interfering signals will exceed that can be handled by the limit mixer's linearity [3].

CMOS technology is preferred to BJT because of lower noise, simpler and lower cost manufacturing. So we use MOSFET cascode structure in order to amplify received signal.

In order to optimize noise figure without affecting the input impedance we use degeneration inductor method which causes to generate a real part in the input impedance of the amplifier [2]. Indeed minimum degeneration inductance in wire bond package can not be lower than 0.5nH [2] so we choose source inductor about 0.8nH.

III. INPUT IMPEDANCE MATCHING

For maximum power transmission from source to the load, input and output of LNA must possess a stable input and output impedance for about 50ohm over the frequency range of interest.

There are a lot of ways for input impedance matching. The first and simplest method is using real resistor. This resistor could have real impedance of 50 ohm in all over the frequency range of interest. But because of high thermal noise of this structure which causes the noise

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figure become more than 6dB, this method is not preferred. Another way of input matching is using common–gate stage. The input impedance of this stage is $1/g_{ms}$. Where g_{ms} is transconductance and would not change a lot in higher frequencies but this structure have a little more noise figure due to using transistor for matching also the gain of this structure isn't so much. Indeed all these structures could design in differential mode in order to cancel common noise of the system. But this structure will occupy more space and increase power dissipation.

Another way of input matching is using noise less components like inductors and capacitances. Some common RLC circuits which are used for impedance matching like L, T and Π models and Impedance Inverting Technique [1] has low noise figure. But they only work in resonance frequency or have the restriction of appearing negative impedance.

For increasing the bandwidth, the matching operation must be done in several steps. In this paper we will introduce a new LC ladder matching network for input impedance matching. The following Fig.1 shows the suggested matching network.

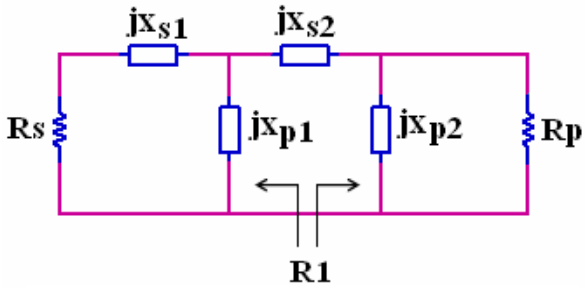

Fig. 1 Two stages LC ladder matching network

We can derive some equations for calculating the value of each Xsn or Xpn (reactive elements). After calculating absolute value for each of them we can replace a capacitor or inductor according to the application of each element. Because of integrated circuit considerations on minimum area occupying, we have to use inductors and capacitors as less as possible, so usually we try to obtain matching requirements by only a two stage ladder network and we provide related equations.

As it's shown in Fig. 2(a), Ladder network is constructed from sub-circuits named L networks; also the matching equivalent of an L network is shown in Fig. 2(b).

If we have a series combination of a resistor Rs and reactance Xs, equivalent impedance Zs and quality factor Qs can be calculated through (1).

$$Zs = Rs + jXs \;\; ; Qs = \frac{|Xs|}{Rs} \qquad (1)$$

The same parameters can be derived for parallel combination of Xp and Rp through (2).

$$Zp = \frac{jRpXp}{Rp + jXp} \;\; ; Qp = \frac{Rp}{|Xp|} \qquad (2)$$

If we want to obtain an equivalent parallel circuit from series or vice versa, we have to apply (3) and (4) for calculating new values,

$$Rs = \frac{Rp}{1+Qp^2} \; ; \; Xs = \frac{Qp^2}{1+Qp^2} Xp \qquad (3)$$

$$Rp = (1+Qp^2)Rs \; ; \; Xp = \frac{1+Qp^2}{Qp^2} Xs \qquad (4)$$

According to definition of the Qs, and set it equal to Qp, we have (5).

$$Qs = \frac{|Xs|}{Rs} = Qp \qquad (5)$$

For the first sub-circuit in Fig. 2(a) we assume thatRp> R1, R1>Rs, Xp1Xs1<0 and Xp2Xs2<0.

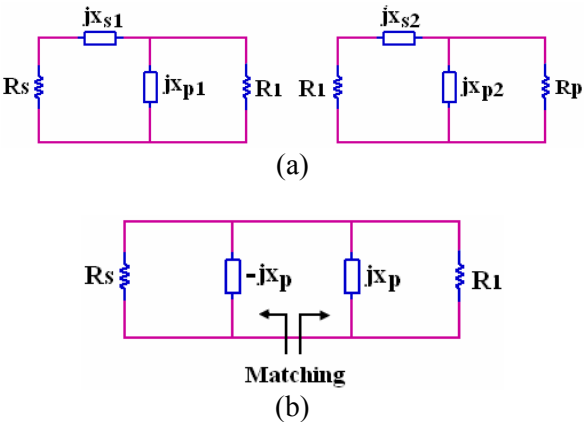

Fig. 2 (a) Illustration of L sub circuits for two stages ladder network. (b) Illustration of matching equivalent for first L sub circuit.

Matching will be occurred if Rs transformed to R1 and Xs1 to –Xp1 (to have conjucated impedances in both sides). Equations (3-5) implies (6) for obtaining conjucation condition.

$$Qs = Qp = \sqrt{\frac{R1}{Rs} - 1} \qquad (6)$$

So we can calculate reactance values through equation (7).

$$|Xs1| = RsQs1; |Xp1| = \frac{R1}{Qp1} \qquad (7)$$

This single stage is able to do the complete matching just in one frequency and the bandwidth is BW=ω0/Qt in which Qt is the total quality factor of the circuit.

$$Qt = \frac{Rp/2}{|Xp|} = \frac{1}{2}Qp = \frac{1}{2}Qs \qquad (8)$$

Right now we can generalize this procedure to more stages and obtain desirable wider bandwidth. For this object we assume R1 as a virtual resistance and couple it to the next L stage this is illustrated in Fig. 1. Related values for two stage ladder is calculated simply by equating quality factor of two consequent L networks and finally results (9).

$$\frac{R1}{RS} = \frac{R2}{R1};\ Q = \sqrt{\frac{R1}{Rs} - 1}$$

$$|XS1| = Q \times RS; |XS2| = Q \times R1 \qquad (9)$$

$$|XP1| = \frac{R2}{Q}; |XP2| = \frac{RS}{Q}$$

Since this matching network is performed to operate as a Band Pass filter and for the biasing consideration, we choose Xp1 and Xs2 as a capacitor and Xs1 and Xp2 as an inductor. Applying capacitor and inductor definition we can find their related values.

$$L1 = \frac{XS1}{2\pi f_0};\ L2 = \frac{XP2}{2\pi f_0} \qquad (10)$$
$$C1 = \frac{1}{2\pi f_0 XP1};\ C2 = \frac{1}{2\pi f_0 XS2}$$

After combining this input matching network with cascode stage, according to Fig. 3, the input impedance of cascode stage presents with (11):

$$Z_{in} = R_{in} + jX_{in} = \frac{g_m L_s}{C_{gs}} + j(\omega L_s - \frac{1}{\omega C_{gs}}) \qquad (11)$$

We can neglect imaginary part of this impedance in resonance frequency. Rp in Fig.1 is equivalent to Rin in equation (11), so we must match impedance of source (Zs=Rs=50Ω) with Rin.

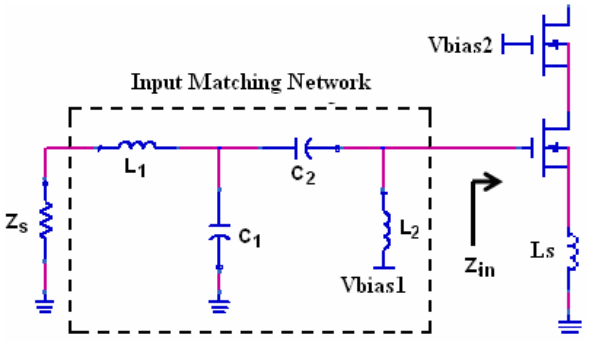

Fig. 3 Input matching

As we choose Ls as 0.8nH, and with help of *gm* and *Cgs* formulas and 0.13µm TSMC technology parameters, Rin will be found through (12).

$$gm = \mu_n C_{ox}(W/L)V_{eff};\ Cgs = \frac{2}{3}(C_{ox}WL)$$
$$Rin = \frac{gmLs}{Cgs} = \frac{3\mu_n V_{eff} L_s}{2L^2} = 93.4\Omega \qquad (12)$$

From equation (9, 10, 12), the values of L1, C1, C2 and L2 are calculated as 0.8nH, 0.235pF, 0.641pF and 4nH respectively.

The cascode size of transistors could calculate simply by paying attention to this point that the imaginary part of Zin must be zero in resonance frequency. Since you choose the value of Ls, Cgs could be found through (13).

$$\omega_c^2 = \frac{1}{L_s C_{gs}} \qquad (13)$$

With help of Cgs formula, W or the size of transistors evaluates. The proper value of W in this structure was 120µm.

IV. Output Impedance Matching

We could use the same input impedance matching technique for output matching. In order to use this method first we must know r_{ds} and C_{ds} of second cascode transistor. r_{ds} is related to λ

parameter which was not obvious in 0.13µm. But a simple way for out put matching is using source follower stage [5]. Output impedance of this stage is simply defined by $1/g_m$. As mentioned before, this parameter couldn't change in higher frequencies so we can have constant output impedance using this approach.

According to value of g_m, current bias and W will choose from (14).

$$gm = \mu_n C_{ox} (W/L) V_{eff} = 2\sqrt{\frac{\mu_n C_{ox} W}{2L} I_D} \quad (14)$$

Fig. 4 shows the overall schematic of designed LNA.

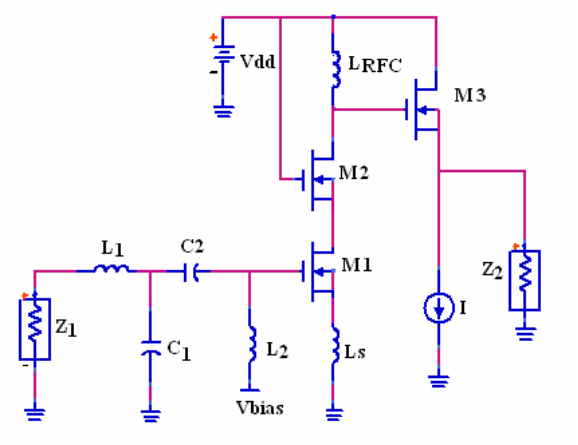

Fig. 4 Overall Schematic of designed LNA

We assume L_{RFC} is equal to 3nH. But It is a trade off in choosing Ls and L_{RFC}; we can reach lower S11 with decreasing the values of Ls while noise figure will increase. Also increasing L_{RFC} will decrease frequency peak of S21.

Simulation results show that with biasing voltage about 0.65v, the current consumption of cascode stage is about 3.92 mA and total power consumption with 1v supply voltage is 8.846mW.

V. Simulation Results

Simulation Results for 0.13µm technology in Full band of UWB are shown in Fig. 5-11.

The noise figure of designed LNA (Fig. 5) is less than 1.75dB due to using noise less components for input impedance matching and shows very good noise performance for Ultra-Wideband LNA.

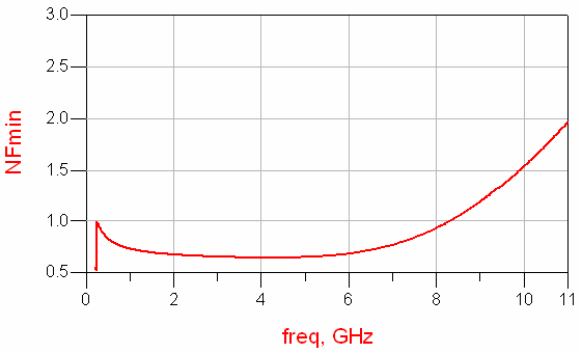

Fig. 5 Noise Figure is less than 1.75dB over the Full band of UWB

S21 which shows the overall gain is more than 10dB in all over the UWB and it reaches to 25dB in middle frequency.

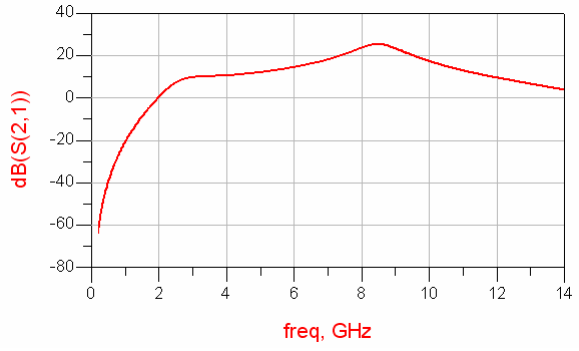

Fig. 6 S21 or Gain is more than 10dB in Full band of UWB

S11 and S22 which show input and output impedance matching are shown in figure 7-10. Simulation results shows S11 below -7dB and S22 less than -10dB in average over the target bandwidth which shows reasonable input and output matching for a systematic approach design.

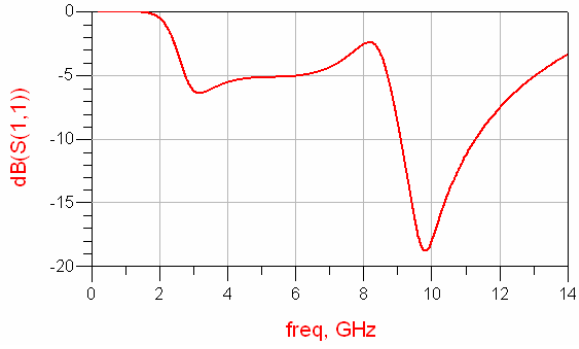

Fig. 7 S11

Also S11 and S22 will be improved by decreasing the value of Ls.

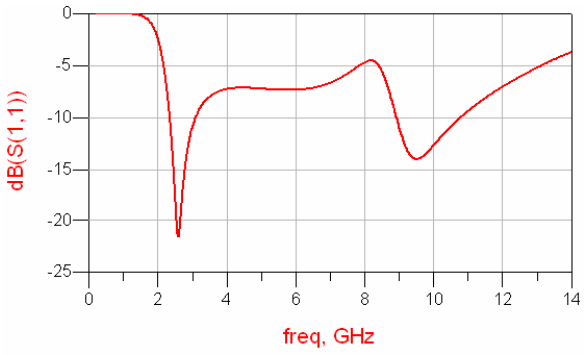

Fig. 8 S11 by decreasing Ls

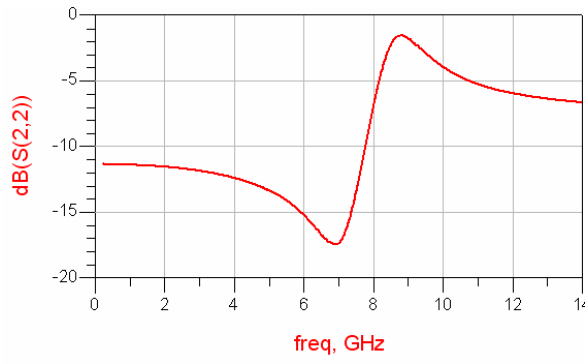

Fig. 9 S22

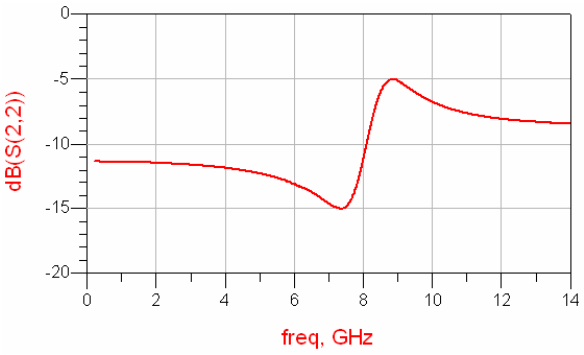

Fig. 10 S22 by decreasing Ls

Since we use cascode architecture S12 is less than -35dB and shows good isolating between input and output of LNA.

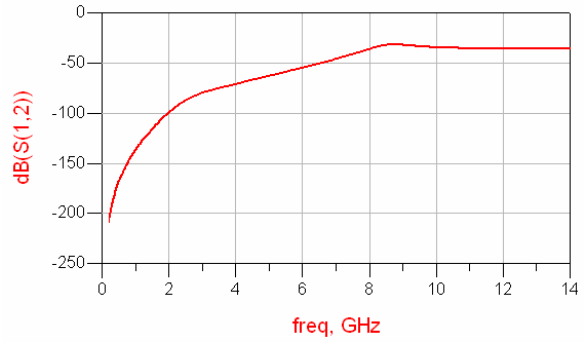

Fig. 11 S12

VI. Conclusion

Based on the theoretical and practical analysis, a systematic mathematical relation based procedure for design of an UWB CMOS LNA presented in this paper. Designed LNA achieves up to 10dB power gain with a suppressed NF less than 1.75dB over the full band of UWB. This systematic approach provides good input and output matching while consuming only 8.846mw with 1V supply voltage.

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References

[1] H. J.Lee, D.S. Ha and S. S. Choi, "A systematic approach to CMOS Low Noise Amplifier design for Ultra Wide Band Applications," *IEEE journal*, 2005.

[2] A. Ismail and A. Abidi, "A 3–10-GHz Low-Noise Amplifier With Wideband LC-Ladder Matching Network," IEEE J.Solid-State Circuits, vol.39, no.12, pp.2269–2277, 2004.

[3] A. Nabavi, course of CMOS Low Noise Amplifier, WWW.MODARES.AC.IR

[4] P. Amiri, A. Nabavi, H. Gharaeei, "A 10 GHz Reconfigurable UWB LNA in 130nm CMOS", Malaysia ICSE2006 Proc.2006.

[5] Z.Amini, S.Choobkar and A. Nabavi, "A Low Noise Amplifier For Ultra-Wide band Systems", in 0.13µm COMS Technology" Faculty of Engineering Tarbiat Modares University. 2006.

[6] F. Kalantari, N. Masoumi, "A Fully Integreated Dual-Band CMOS LNA for IEEE802.16a", IEICE Electronics Express J.Solid-State, 2006.

[7] B Behzad Razavi, "RF microelectronics", Prentice-Hall, Inc., Upper Saddle River, NJ.