A Low-Jitter PLL Clock Generator for Microprocessors with Lock Range of 340–612 MHz

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***Abstract*— A fully integrated, phase-locked loop (PLL) clock generator/phase aligner for the POWER3 microprocessor has been designed using a 2.5-V, 0.40-μm digital CMOS6S process. The PLL design supports multiple integer and noninteger frequency multiplication factors for both the processor clock and an L2 cache clock. The fully differential delay-interpolating voltage-controlled oscillator (VCO) is tunable over a frequency range determined by programmable frequency limit settings, enhancing yield and application flexibility. PLL lock range for the maximum VCO frequency range settings is 340–612 MHz. The charge-pump current is programmable for additional control of the PLL loop dynamics. A differential on-chip loop filter with common-mode correction improves noise rejection. Cycle–cycle jitter measurements with the microprocessor actively executing instructions were 10.0 ps rms, 80 ps peak to peak (P-P) measured from the clock tree. Cycle-cycle jitter measured for the processor in a reset state with the clock tree active was 8.4 ps rms, 62 ps P-P. PLL area is 1040 × 640 μm^2. Power dissipation is <100 mW.**

***Index Terms*— Clock generator, clocking, microprocessors, phase-locked loop (PLL).**

I. Background

THE use of phase-locked loops (PLL) for generating phase-synchronous, frequency-multiplied clocks in microprocessors has been prevalent in industry [1]–[4]. In recent years, the trend toward ever increasing clock frequency has made PLL's even more attractive due to the difficulties in distributing high-frequency clocks through several levels of packaging [5], [6], but the jitter penalty for using a PLL has not kept pace with the rate of reduction in processor cycle time. Until this year,[1] the best reported microprocessor PLL jitter penalties ranged from 82 to 83 ps peak to peak (P-P) for inactive processors [1], [5], and a PLL on a small (600-K transistor) graphics display chip has been reported with 80 ps P-P jitter for a quiet supply at 320 MHz [7]. Many examples of higher jitter PLL designs exist in the literature. Power-supply noise created from the digital switching activity on a microprocessor is recognized as a major source of PLL jitter, and the primary focus of designers has been directed toward reducing this sensitivity.

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[1]Recent announcements of a 1-GHz microprocessor PLL [12], [13] and a PLL with an on-chip regulator [14] reported jitter of $<\pm 9$ ps (quiet conditions)/$<\pm 36$ ps (processor active) and $<\pm 10$ ps (sinusoidal external noise)/$<\pm 20$ ps (square wave external noise), respectively.

II. Introduction

This paper describes a fully integrated PLL-based clock generator/phase aligner used for the POWER3 microprocessor. The microprocessor is fabricated in IBM CMOS6S technology and contains approximately 12 million transistors. With the microprocessor actively executing instructions, this PLL achieved cycle–cycle jitter of 10.0 ps rms, 80 ps P-P in its application environment and 8.4 ps rms, 62 ps P-P with the microprocessor in a reset state with a portion of the clock tree active.

A simplified block diagram of the PLL clock generator is shown in Fig. 1. The external reference or BUSCLK enters a receiver and is divided by two by divider stage M_1 before entering the phase/frequency detector (PFD) as Φ_i. The internal feedback signal Φ_o from divider M_6 is compared to Φ_i by the PFD, which generates an error signal Φ_e, which is used by the charge-pump and filter network to control the voltage-controlled oscillator (VCO). The output frequency of the VCO is divided by M_3 and is used as the main processor clock (PCLK) after passing through four levels of clock buffering in an H-tree clock distribution network. The processor clock is passed through a delay-matching receiver before entering divider M_6, completing the feedback path. Since at equilibrium the inputs of the PFD will be matched in frequency (and phase), the processor-to-bus frequency ratio is equal to the ratio $f_{P\mathrm{CLK}}/f_{\mathrm{BUS}}$, which is equal to the ratio M_6/M_1, allowing integer or noninteger frequency synthesis by changing divider ratios. Since the technique does not require clock choppers [2], the duty cycle and phase alignment are relatively insensitive to environment and process tolerances. The output of the VCO is also connected to frequency divider M_5, which is used for the L2 cache clock (L2CLK). Since $f_{\mathrm{VCO}} = M_3 \cdot f_{P\mathrm{CLK}} = M_5 \cdot F_{L2\mathrm{CLK}}$, the processor-to-L2 clock-frequency ratio is also adjustable to integer or noninteger ratios. Other phase-synchronous clocks may be designed in similar fashion, and quadrature or interstitial clocks may be created by a polarity change at the divider input. Using the structure of Fig. 1, the VCO frequency f_{vco} is equal to M_3 times the processor clock frequency $f_{P\mathrm{CLK}}$. For cases when M_3 is even, the processor clock edges are generated from only one VCO clock edge; hence a nearly ideal 50% processor clock duty cycle may be achieved through its independence from the VCO duty cycle.

III. Process Technology

The microprocessor and integral clock generator PLL are fabricated in a five-layer CMOS process with 0.4-μm feature

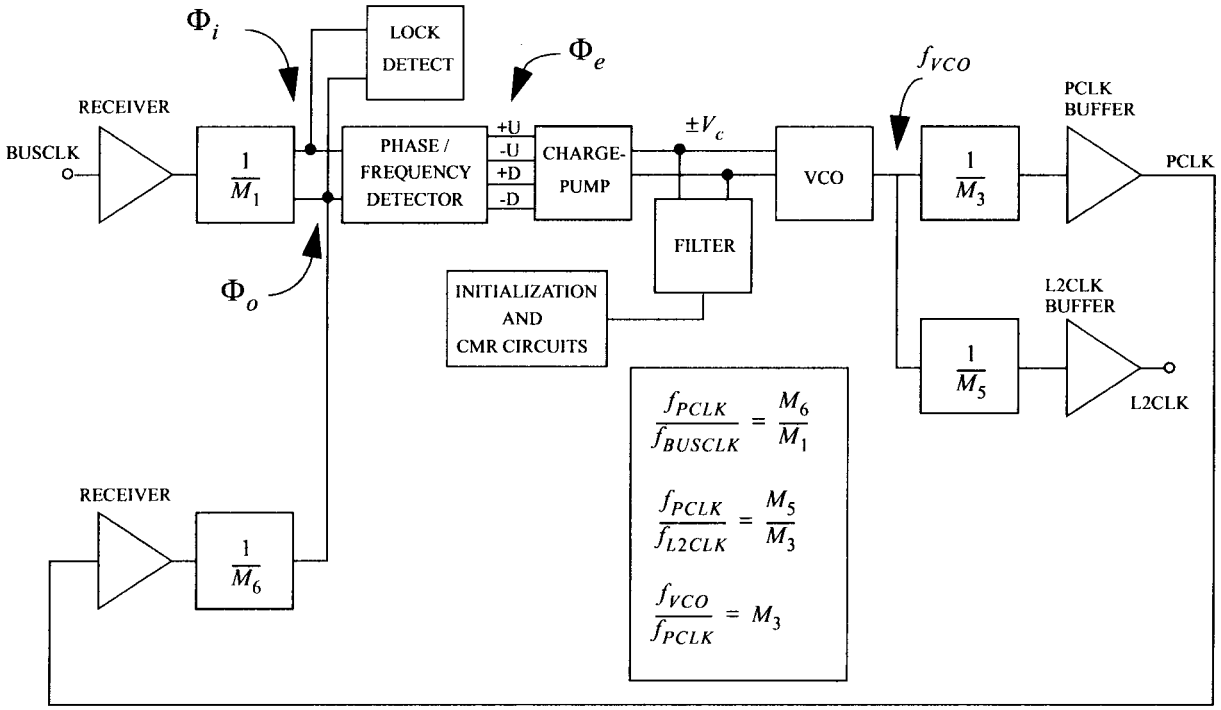


Fig. 1. PLL block diagram.

TABLE I
CMOS6S PROCESS SUMMARY

Minimum lithographic image	0.3 μm
Supply Voltage	2.5 V
N-well / P-epi on P+ bulk substrate	
Leff	0.200 μm
Tox	5.5 nm
Idsat	552 (n) 254 (p) μA/μm
Vt	0.5 V
5 metal levels + local interconnect	
M1 pitch	1.12 μm
M2-4 pitch	1.44 μm
M5 pitch	3.84 μm

sizes. Table I lists some of the relevant attributes of this process technology.

The PLL clock generator is shown in the microprocessor die photograph of Fig. 2(a). The dimensions of the entire PLL are 1040 × 640 μm^2. It is shown with the major features identified in Fig. 2(b).

IV. PLL CLOCK GENERATOR COMPONENTS

A. Phase/Frequency Detector

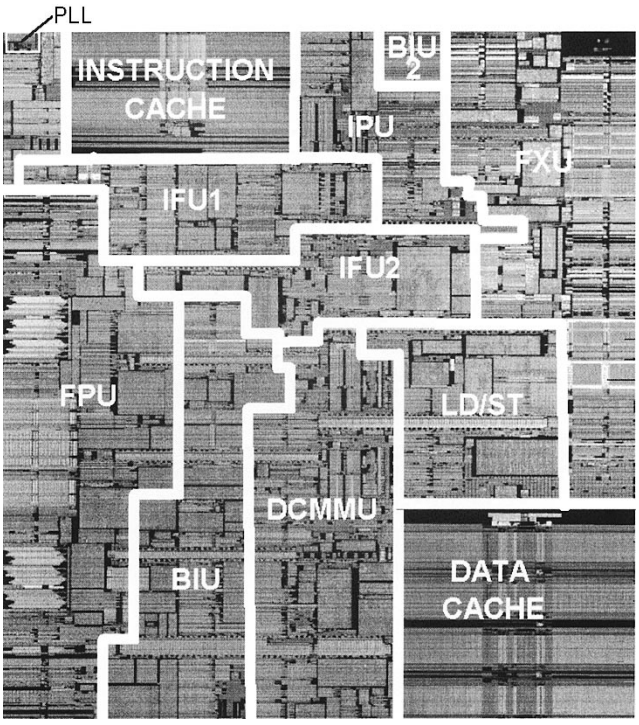
The digital PFD generates a signal that conveys relative phase and frequency error information about its inputs to the charge pump and filter. The PFD design is based on a three-state machine structure [8], as depicted in Fig. 3(a). From the initial reset state, a rising edge on the Φ_i input will assert the +UP output until the rising edge of Φ_o appears, which deasserts +UP and forces a reset of both flip-flops [Fig. 3(b)]. A rising edge first appearing on Φ_o similarly asserts +DOWN until a rising edge arrives at Φ_i, followed by a subsequent reset. Complementary outputs are generated by the PFD for use in the differential charge-pump stage that follows the PFD. The pulse width of the output varies proportionally with the phase error between the two inputs, except for the dead-zone region as the difference approaches zero. This dead zone exists when the phase error becomes small relative to the combined response time of the PFD, charge pump, and filter circuits. Circuit simulation results show a nominal dead zone of ±25 ps. Concerns of current mismatch in the charge-pump and filter networks are reduced at the expense of increased dead zone by preventing simultaneous assertions of +UP and +DOWN.

B. Power-Supply Isolation

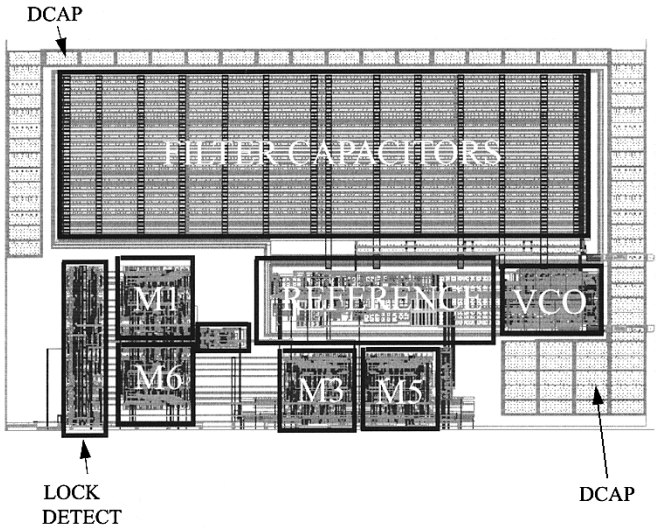
A separate analog power connection (AVDD) is used for the analog circuits [current reference, charge pump, common-mode rejection (CMR), filter initialization, and VCO circuits] to increase the isolation of the sensitive circuits from the logic-induced switching noise present on the main power supply. To allow the detection of potential defects using conventional testing, the AVDD pin is held low, disabling the analog devices that normally draw dc current. Both on-chip and on-module decoupling is used on AVDD.

C. Reference Circuit

A thermal voltage-referenced current source is used to provide temperature- and supply-independent biasing for the analog circuits in the PLL. The circuit contains an array of P+ diffusions in the N-well connected to form two forward-biased diodes with areas that differ by a factor of ten. When connected

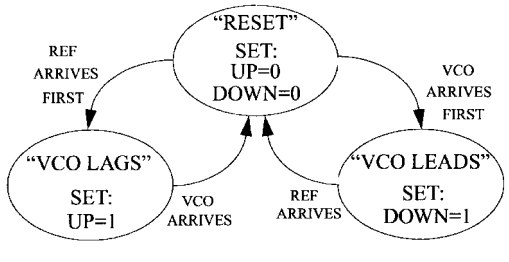


(a)

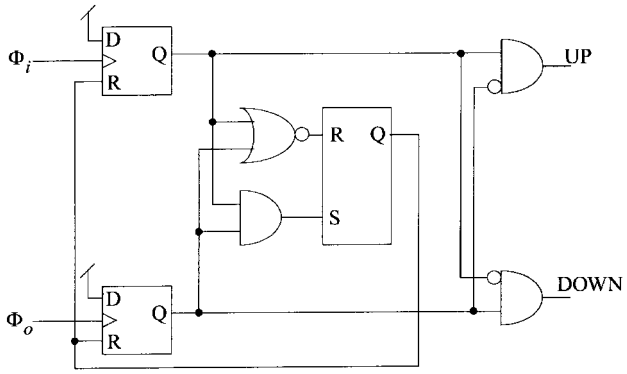


(b)

Fig. 2. (a) Die photograph of POWER3 microprocessor. (b) PLL layout.



(a)



(b)

Fig. 3. (a) PFD state diagram. (b) Phase detector implementation.

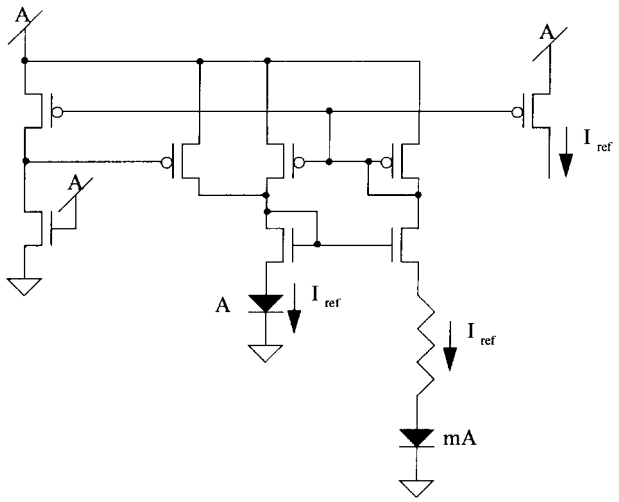
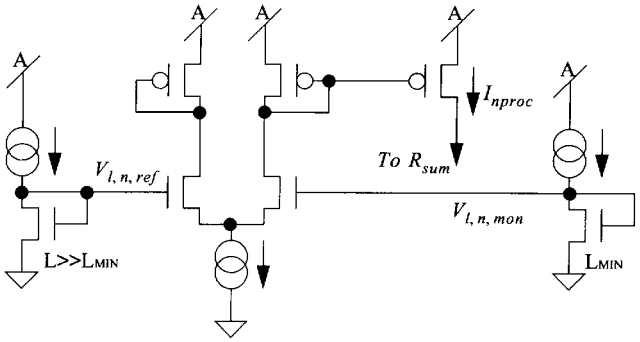


Fig. 4. Reference circuit.

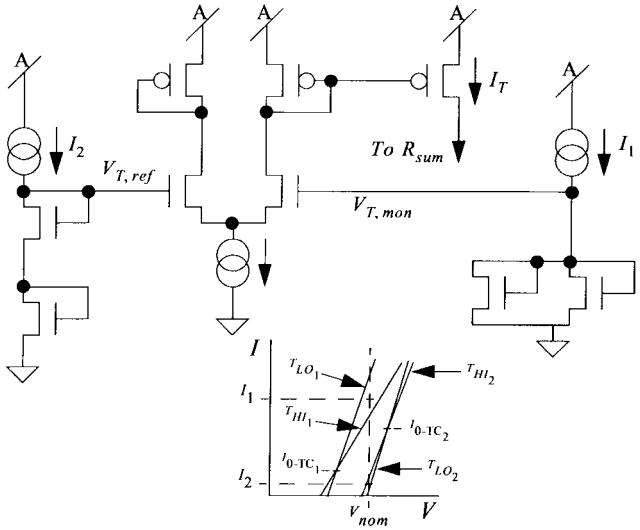
as shown in Fig. 4, the current $I_{\rm ref}$ through each leg has two stable operating points, $I_{\rm ref} = (kT/q)\,(\ln(10)/R) = 10.6\ \mu$A or $I = 0$. The startup circuit prevents the zero current state from occurring by injecting current into one leg during initial power-on. The resistor is implemented using the precision resistor available in the process, which has a temperature coefficient (TC) of +2000 ppm/°C. The positive TC's of the thermal voltage term and the resistor tend to cancel, providing a reference current TC of +785 ppm/°C at 85°C. The reference current $I_{\rm ref}$ is used for subsequent generation of reference currents and the PMOS bias voltage V_p through mirroring. Sensitivity to power-supply change is +1.7%/V for ±20% change on VDD.

D. Process and Temperature Compensation

Variations in $L_{\rm eff}$ due to process are monitored using the circuit shown in Fig. 5(a). All of the current sources are generated directly from the reference circuit current $I_{\rm ref}$. A constant current is passed through a branch containing short-channel NMOS devices, creating a monitoring voltage $V_{t,n,\rm mon}$, which is sensitive to NMOS device length variations. This voltage is compared to a reference voltage $V_{t,n,\rm ref}$ generated by a constant current through a long-channel NMOS device that is relatively insensitive to length variations. The devices and bias currents used for length sensing are sized so that $V_{t,n,\rm mon}$ and $V_{t,n,\rm ref}$ are equivalent for a nominal $L_{\rm eff}$ process. To minimize temperature sensitivity, the bias currents correspond to the zero-temperature coefficient (0-TC) region of the devices.



(a)



(b)

Fig. 5. (a) Process compensation circuit. (b) Temperature compensation circuit.

The two voltages are compared using a differential amplifier, which generates a current proportional to the NMOS L_{eff} offset from nominal. This current is mirrored to produce a current $I_{n\text{proc}}$ that is injected into a precision resistor R_{sum} used for combining various process monitors to generate a compensating reference voltage. The compensating reference voltage is connected to the active load elements of the VCO, which control the VCO's voltage swing. A current $I_{p\text{proc}}$ generated from a similar PMOS circuit also is injected into the resistor.

Weighted combinations of standard bias circuits with differing voltage and temperature coefficients have been used previously to compensate reference circuits for VCO's [9]. In this case, however, temperature was monitored directly by comparing the voltage of two series-connected devices biased by current I_2 below their 0-TC operating point to the voltage of two parallel devices biased by current I_1 significantly above their effective 0-TC point [Fig. 5(b)]. The devices and bias currents are sized so that both branches of the differential amplifier are balanced at V_{nom} for nominal temperature conditions. The inset shows the I–V characteristics as a function of temperature for the series (subscript 2) and parallel (subscript 1) connected devices; the 0-TC points correspond to the crossing point where the current is

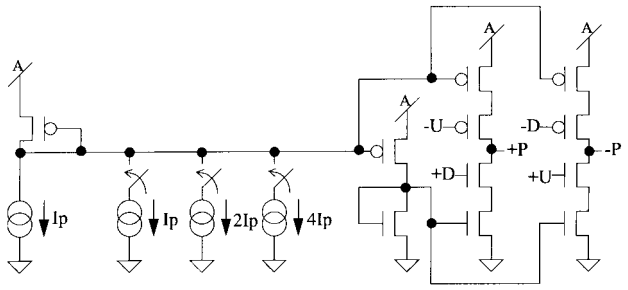


Fig. 6. Charge-pump circuit.

invariant with temperature. The current in one leg of the differential amplifier varies proportionally with temperature and is mirrored and added to the summing junction of the resistor R_{sum}. A constant bias current is also added to the summing junction to establish the correct weighting of the various compensating currents and to correct for the TC of the summing junction resistor.

Using a statistical process model, the process compensation was designed to favor the stabilization of the "best case" side of the distribution over the "worst case" side in anticipation of future process trends. Given the limited range over which a circuit may be practically compensated, the performance for the "best case" devices was not sacrificed at the expense of extensive compensation of the poorest performing devices. For the unsorted population, this approach allowed a reduction in the sensitivity of the VCO to process variability by a factor of 3.6 (55.4–15.2%) over the uncompensated VCO; temperature sensitivity was reduced by a factor of 4.7 (38.6–8.2%).

E. Charge Pump

The reference circuit is used to generate the currents $I_p, 2I_p$, and $4I_p$ for use within the charge pump. The peak charge-pump current may be adjusted in 30-μA increments from 30 to 240 μA by scaling the mirror currents as shown in Fig. 6. The error signals $\pm U$ and $\pm D$ generated by the PFD are used to switch the peak current selected. Adjusting the charge pump allows for optimization of the loop characteristics for different divider and VCO settings. Differential outputs $+$P and $-$P are included for high CMR in the subsequent analog circuits.

F. Loop Filter

The differential loop filter and initialization circuits are shown in Fig. 7. Currents to and from the charge-pump circuit enter the filter at nodes $+$P, $-$P. The input to the filter contains NMOS transmission-gate clamping devices to limit the maximum filter voltage to $AVDD - V_{\text{tn}+}$, where $V_{\text{tn}+}$ is the NMOS threshold voltage for a large source-bulk voltage. For the CMOS6S process, the clamps prevent the filter voltage from exceeding approximately 1.8 V, eliminating concern for the VCO input stage's shutting off. The filter capacitors are accumulation-mode gate-oxide devices, and are interleaved to improve the matching. Both loop-filter capacitors together occupy an area of approximately 865 $\times$ 280 μm^2 and are approximately 450 pF each. Precision resistors (1.2 KΩ each) are used to produce a zero in the filter transfer function.

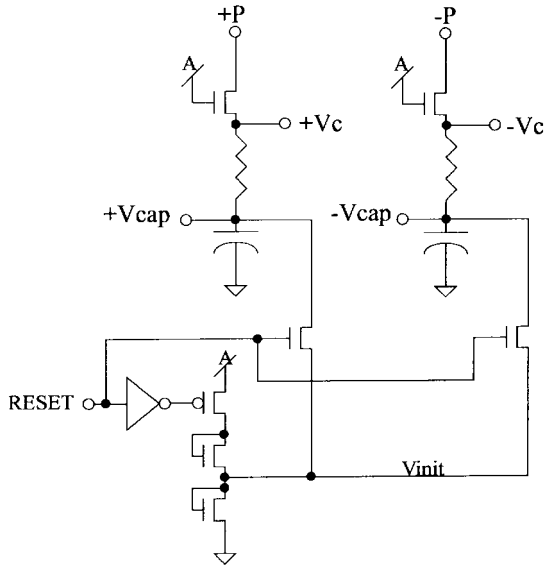


Fig. 7. Loop filter and filter initialization.

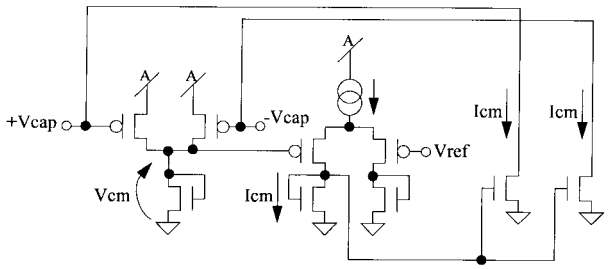


Fig. 8. Common-mode control.

The filter output is connected to the VCO control input at nodes $+V_c, -V_c$. An initialization circuit activated during the initial system power-on-reset is used to precharge the filter capacitors to the nominal common-mode voltages at nodes $+V_{\rm cap}, -V_{\rm cap}$.

G. Common-Mode Control

It is possible for common-mode voltages to develop in the filter from leakage, drift, or device mismatch. Since the common-mode voltage can introduce frequency offsets in the VCO or even inhibit operation for extreme cases, the circuit shown in Fig. 8 was used in conjunction with the filter clamps described earlier. The common-mode voltage of the filter is sensed by generating currents proportional to $+V_{\rm cap}$ and $-V_{\rm cap}$ and summing them across a load device to produce $V_{\rm cm}$. A differential amplifier compares $V_{\rm cm}$ to a reference voltage and generates a current $I_{\rm cm}$, which is proportional to the common-mode voltage. The current $I_{\rm cm}$ is mirrored by two identical current sources, which bleed current from both filter capacitors simultaneously without affecting the differential voltage between them. The maximum drain currents for this structure, which corresponds to the case when both clamps have activated, are approximately 16 μA. For typical cases where the common-mode voltage is below 600 mV, the bleed currents are <1 μA. Stability of the network is assured by heavy dominant-pole compensation.

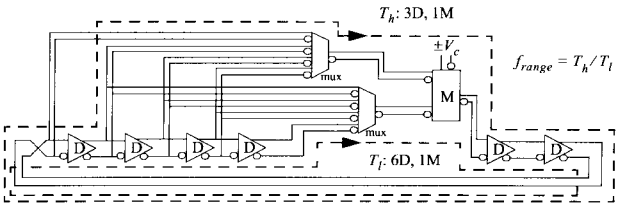


Fig. 9. Voltage-controlled oscillator.

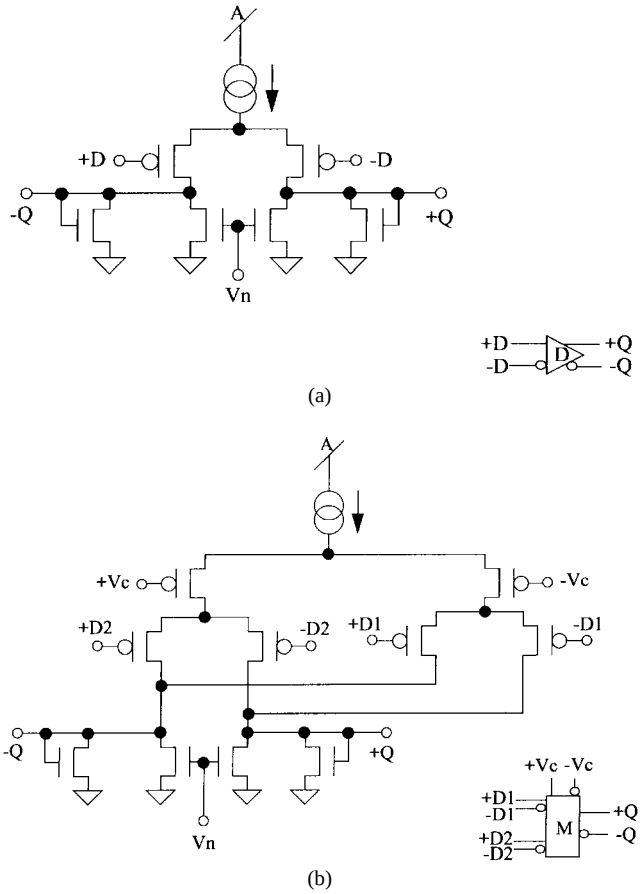


Fig. 10. (a) Delay element. (b) Mixer circuit.

H. Voltage-Controlled Oscillator

The VCO design is based upon a delay-interpolating ring oscillator structure [9]–[11], as shown in Fig. 9. In contrast to the current-starved and current-modulated VCO's, which are very commonly used for microprocessor clock generators, delay-interpolating VCO's have relatively low-to-moderate VCO gains and are well suited to fully differential control and signal path circuit implementations. The lower VCO gain of the delay-interpolating VCO's produces significantly less jitter due to coupled noise than higher gain structures. The limited operating frequency range for delay-interpolating VCO's, which must be less than 2 : 1 to ensure monotonicity, may be effectively augmented by selecting suitable divider ratios or by adding programmability to the VCO signal paths.

The frequency limits of the VCO are determined by the longest and shortest path delays through the structure. Fig. 9 shows an example high-frequency limit of period T_h composed of three delay units and one mixer unit, and a low-frequency

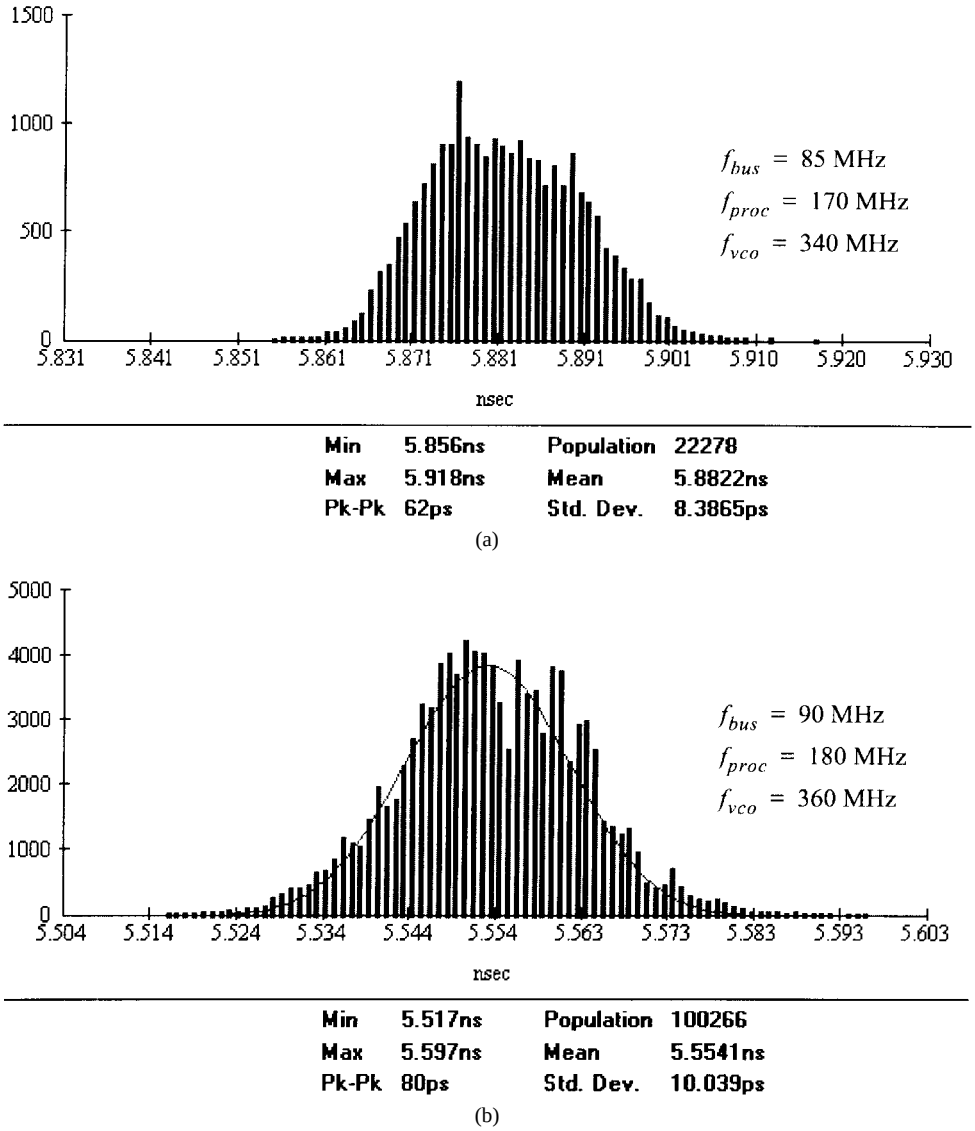


Fig. 11. Cycle–cycle processor clock jitter: (a) quiet processor and (b) active processor.

limit of period T_l composed of six delay units and one mixer unit. These frequency limits also affect the VCO gain (for a given mixer design) as well as the center frequency. The frequency limits may be independently controlled using the multiplexers shown in Fig. 9, allowing flexible control of the VCO operating range and greater than ten-to-one adjustment range for VCO gain.

The delay elements and mixer designs are based upon PMOS source-coupled pair differential amplifiers with NMOS load networks [Fig. 10(a) and (b)] which allow voltage-controlled swing adjustment through effective load-line translation by adjusting the voltage V_n. The high impedance provided by the current source improves the supply noise rejection for the source-coupled pair, and the N-well improves the isolation to the p+ bulk substrate noise. The variation of the threshold voltage due to bulk effect is eliminated using bulk-to-source biasing throughout the structure. Sensitivity of the VCO to low repetition rate, 100-mV steps on VDD and AVDD is 0.418 ps/mV. Center-frequency common-mode voltage sensitivity is <3.5% over the full input range dictated by the common-mode control circuit. Nominal VCO gain for the settings that produce the maximum VCO range is 185 MHz/V. The worst case VCO power dissipation is 30 mW.

I. Dividers and Receivers

Dividers M_1, M_3, M_5, and M_6 (Fig. 1) may be individually programmed and support division by 2, 3, 4, 5, 6, 8, or 10. The dividers are placed in pairs within the layout to improve device matching between M_3 and M_5 and between M_1 and M_6. The receivers shown in Fig. 1 are also placed together and are located near the I/O pad for BUSCLK.

V. PLL Measurements

The damping factor, loop gain, and natural frequency of the PLL may be adjusted over a wide range to match the application by changing the charge-pump and VCO gain as described above. System testing was conducted with 90-A peak charge-pump current using the maximum frequency and range on the VCO with a variety of divider settings and BUSCLK

frequencies. The processor clock was accessed from the clock tree through a series of inverters. A time-interval measurement (TIM) system was used to measure cycle–cycle period jitter statistics for a number of packaged die representing various process skews. The processor was operated using an array initialization program loop with the fixed-point and floating-point processors active for the "active" processor tests, and was also operated in a "quiet" mode reset state. All tests were performed at room temperature with ambient forced-air cooling. Conventional first-cycle oscilloscope-based jitter measurements were performed periodically and provided P-P jitter results that were consistent with those measured on the TIM system. The external clock was provided by a high-frequency pulse generator, with 7.3 ps rms, 36 ps P-P jitter.

Fig. 11(a) shows a histogram of cycle–cycle period measurements taken with the processor in an inactive reset state but with the clock tree active. The frequencies of the reference clock, processor clock, and VCO are 85, 170, and 340 MHz, respectively, which corresponds to a -3-dB loop bandwidth of 2 MHz. The distribution of samples in the histogram follows a Gaussian distribution with period jitter of 8.4 ps rms, 62 ps P-P. The minimum period measured for this sample size $(n = 22\,278)$ was 26.2 ps less than the mean (3.1 sigma away). Assuming that cycle-time failures only occur on the minimum period side, the worst case clock jitter penalty for this system (i.e., a "quiet" processor) is 26.2 ps at 3.1 sigma confidence (or 25.2 ps penalty at 3.0 sigma). Since a peak-to-peak jitter approximately equal to the PFD dead zone can exist for the PLL, the ± 25 ps simulated value for the dead zone may be a significant component of the measured jitter.

Fig. 11(b) shows a clock-jitter histogram for the processor executing the array initialization routine for a large population $(n = 100\,266)$. A Gaussian curve has been superimposed on the histogram for comparison purposes. The frequencies of the reference clock, processor clock, and VCO are 90, 180, and 360 MHz, respectively. For this system (i.e., an "active" processor), the period jitter has increased to 10.0 ps rms, 80 ps P-P, and the worst case clock-jitter penalty is 37.1 ps at 3.7 sigma confidence (or 30.1 ps at 3.0 sigma). The effective noise penalty for running the array initialization routine is 4.9 ps at 3.0 sigma.

VI. Conclusion

This work demonstrates the viability of a low-jitter PLL design approach amenable to high-speed microprocessors. Measured jitter for the design was 8.4 ps rms, 62 ps P-P for quiet conditions and 10.0 ps rms, 80 ps P-P for the processor active. A tunable, moderate-gain VCO with active process and temperature compensation provides high power-supply rejection and low sensitivity to temperature and process variability. A differential design approach maintains noise immunity in both control and signal paths within the analog portions of the PLL.

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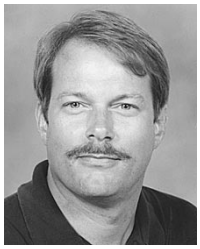

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